

FIG. I

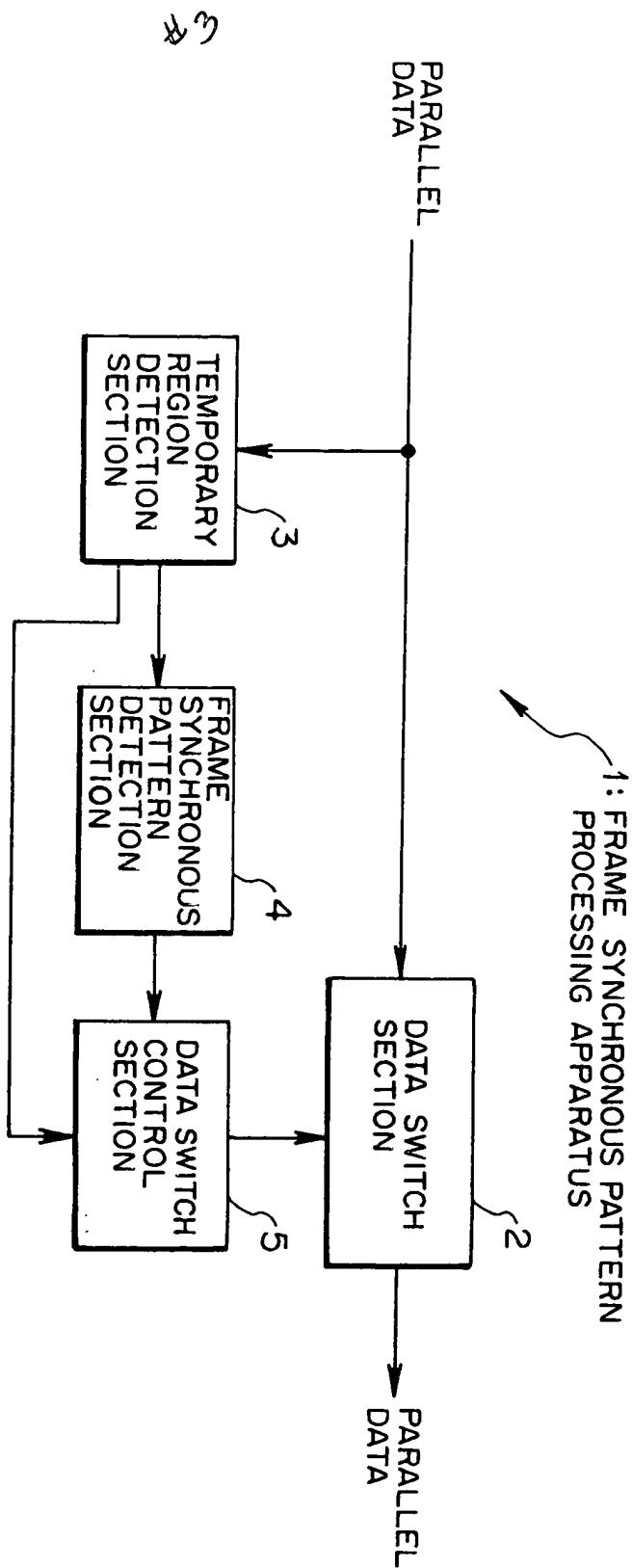


FIG.2

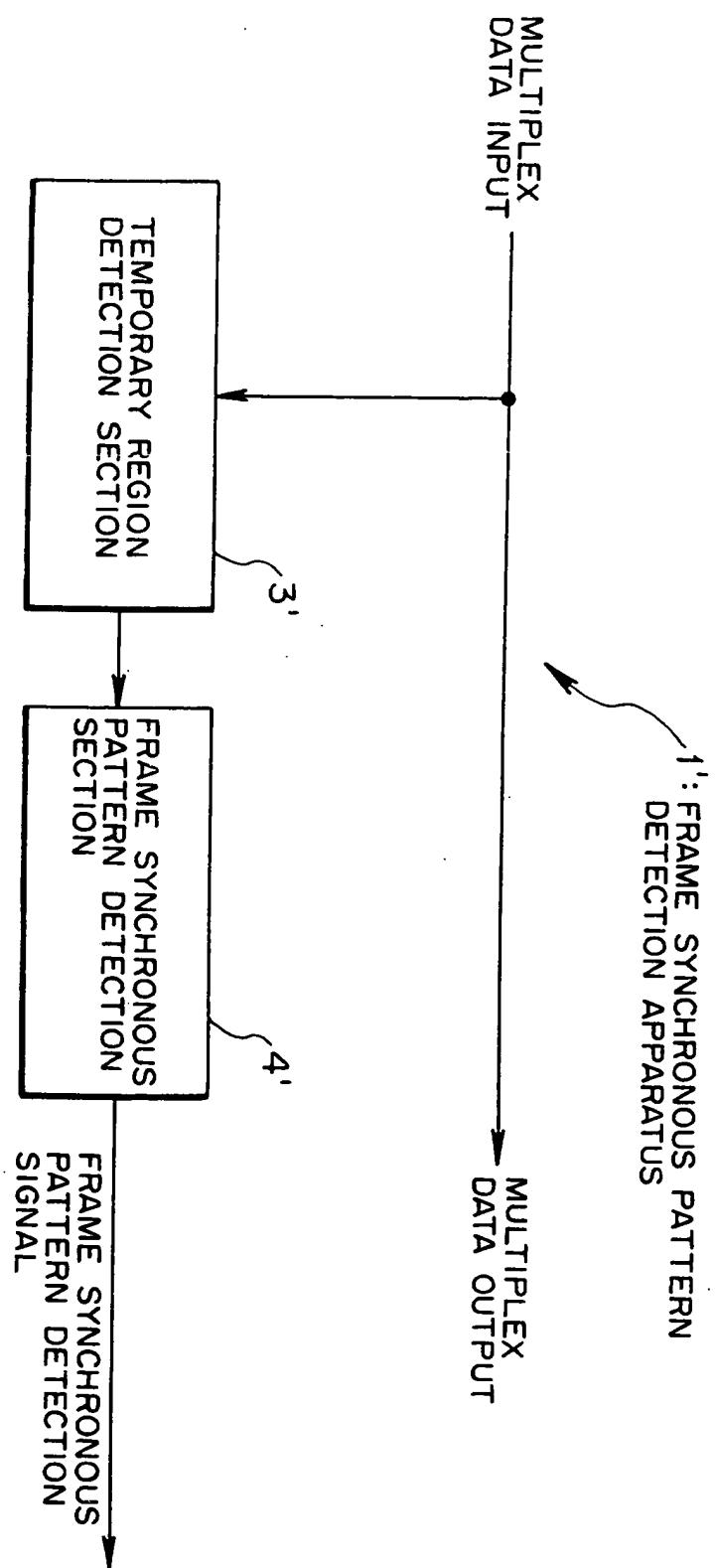


FIG.3

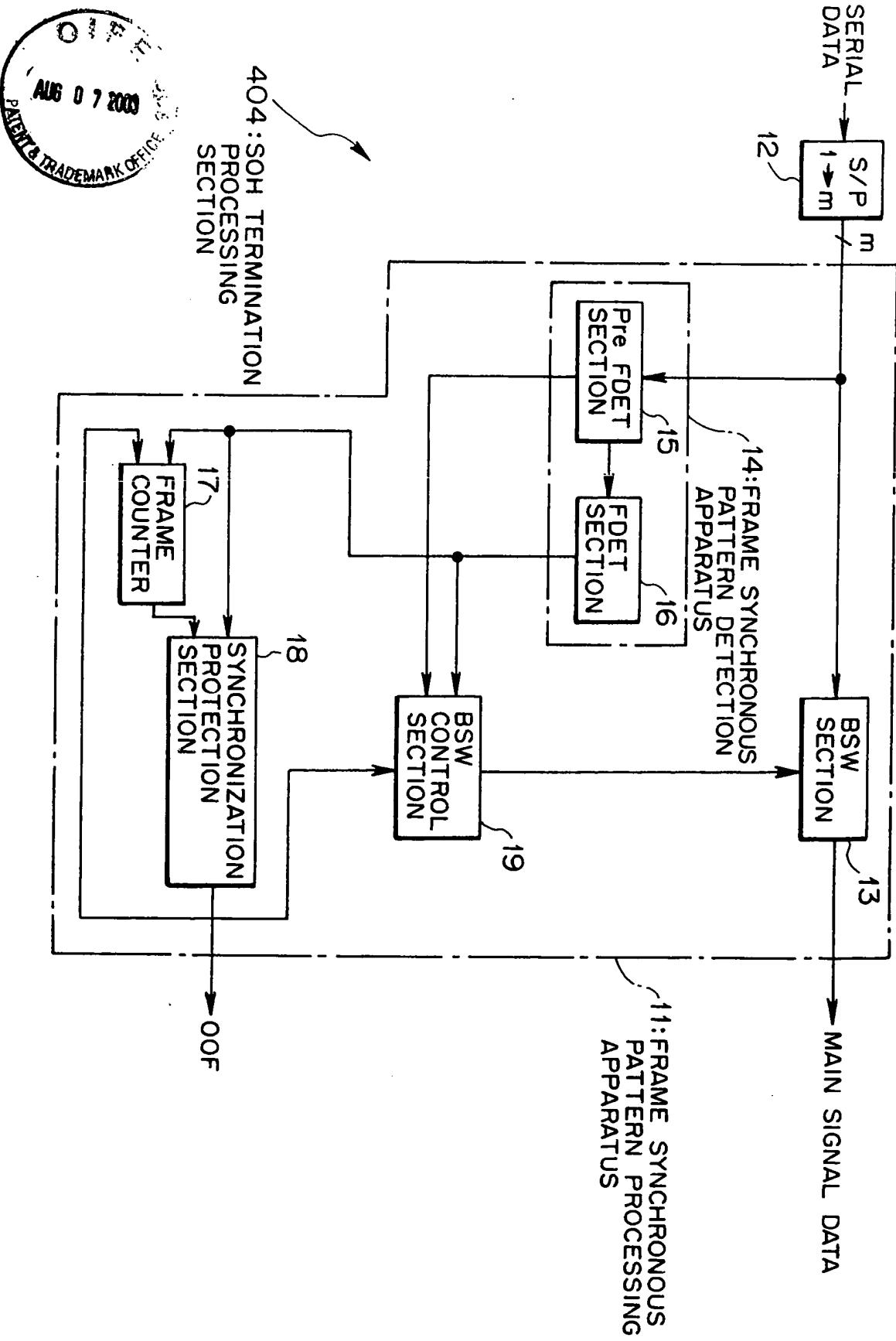


FIG. 4

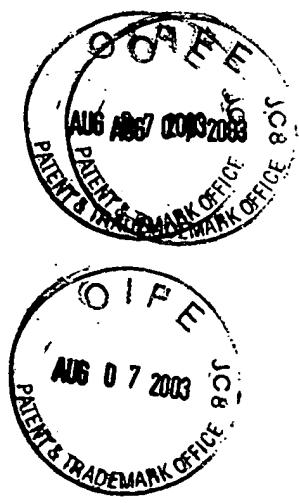
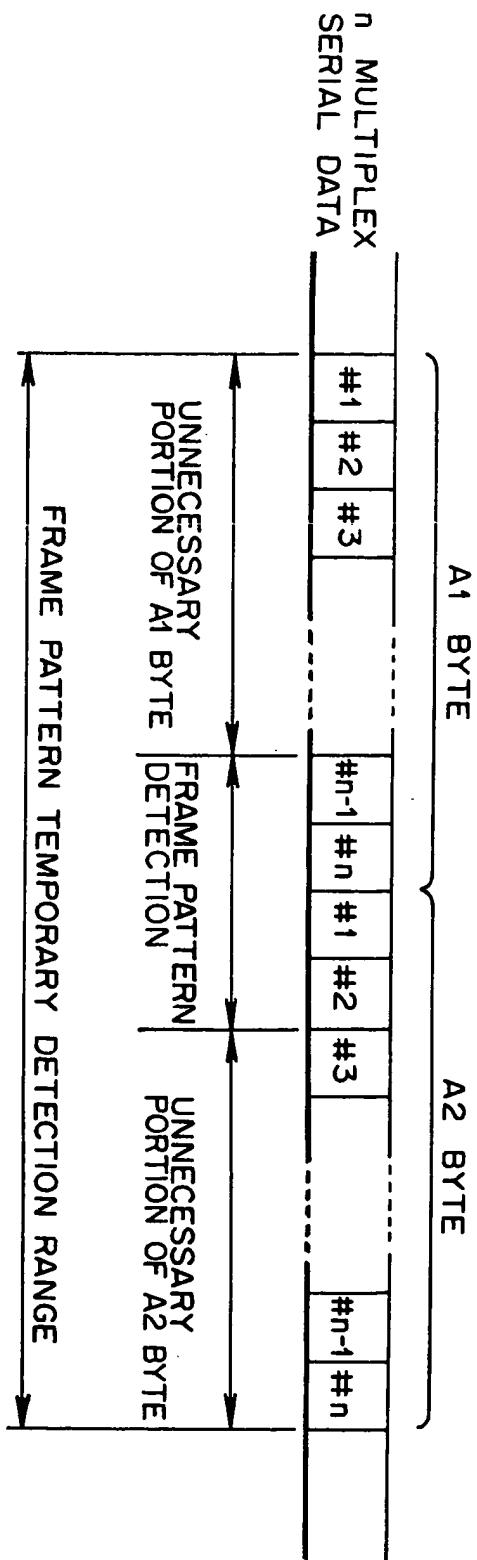


FIG.5

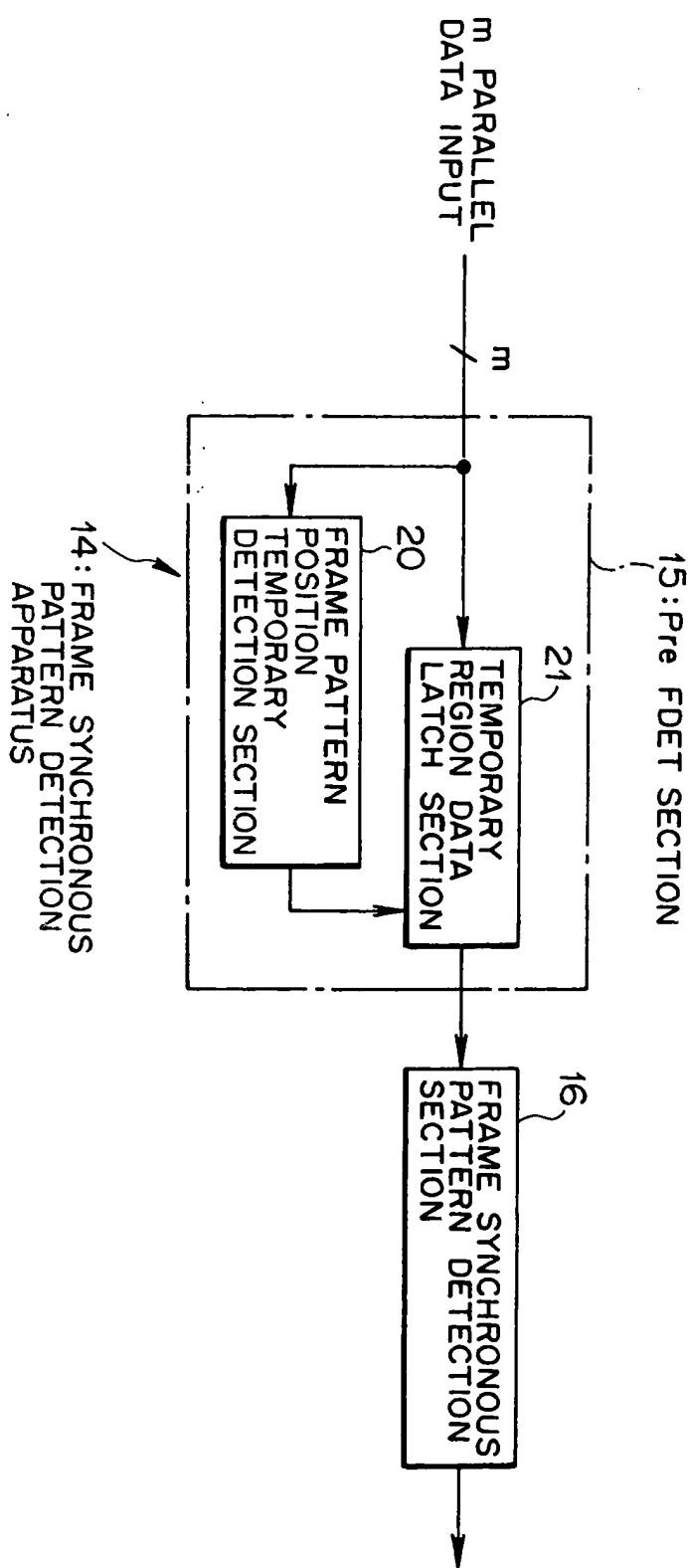


FIG. 6

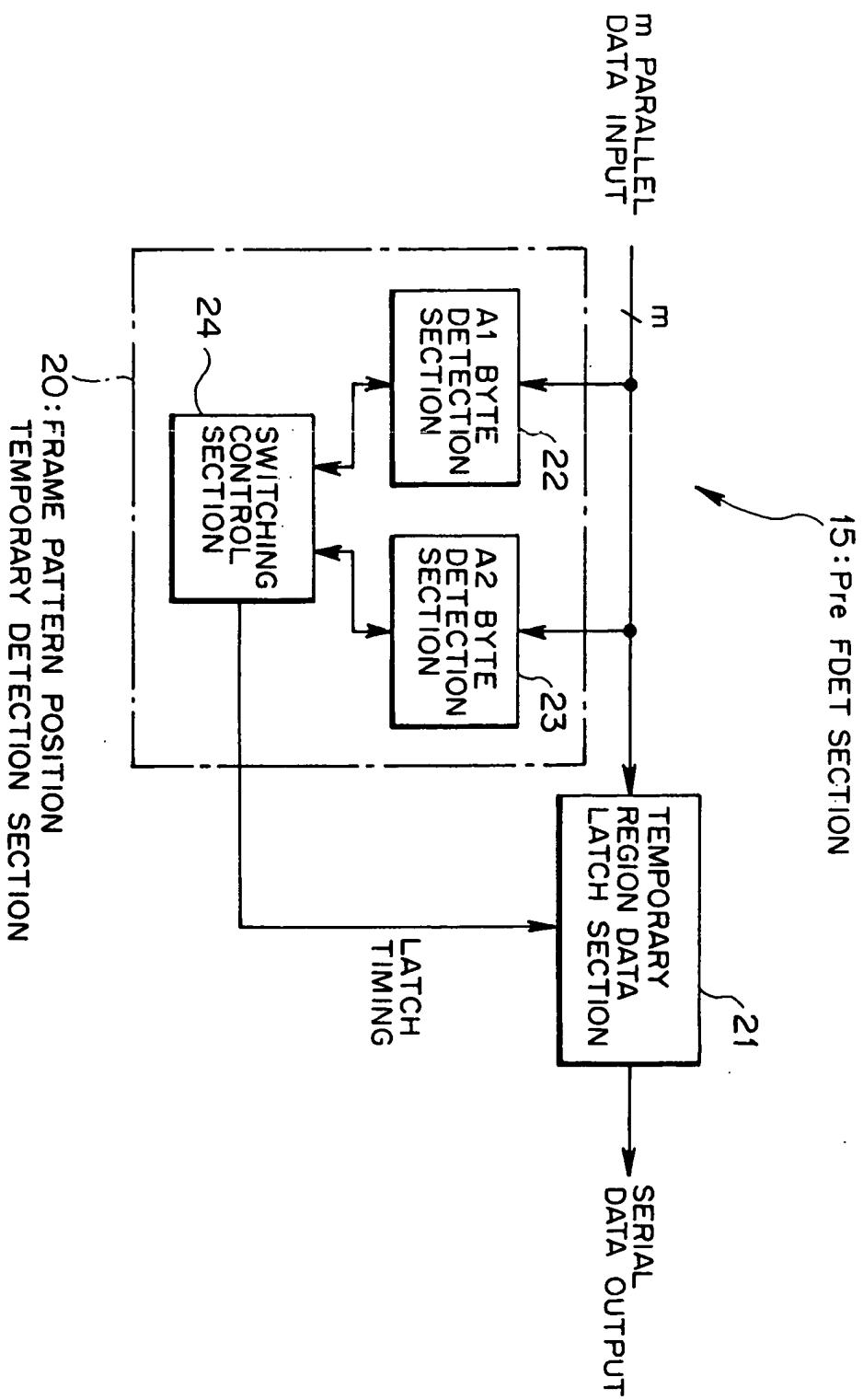
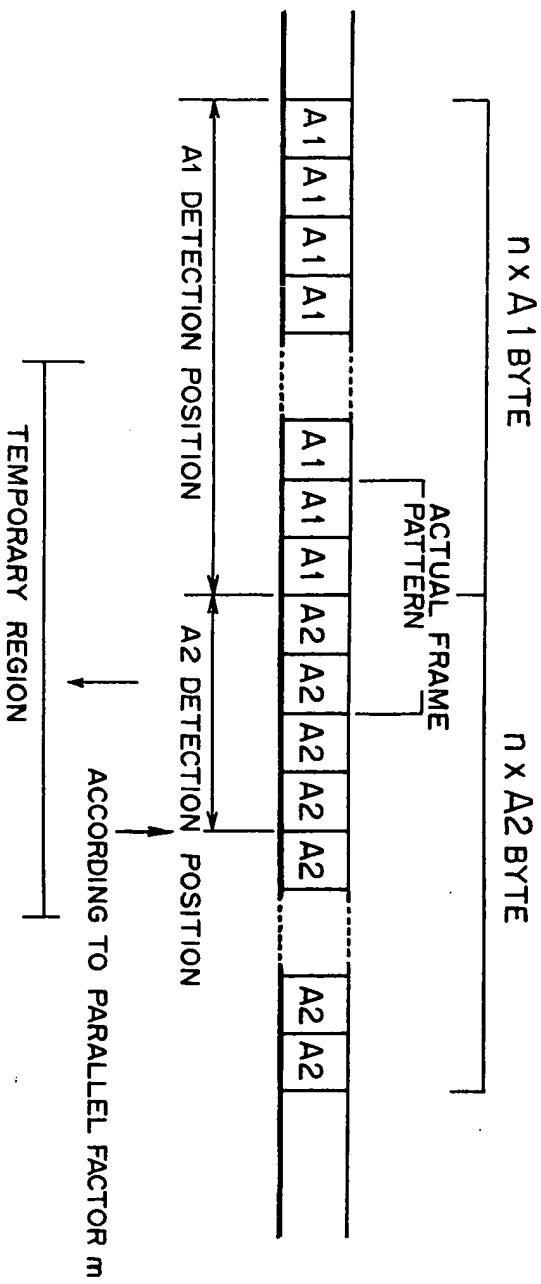


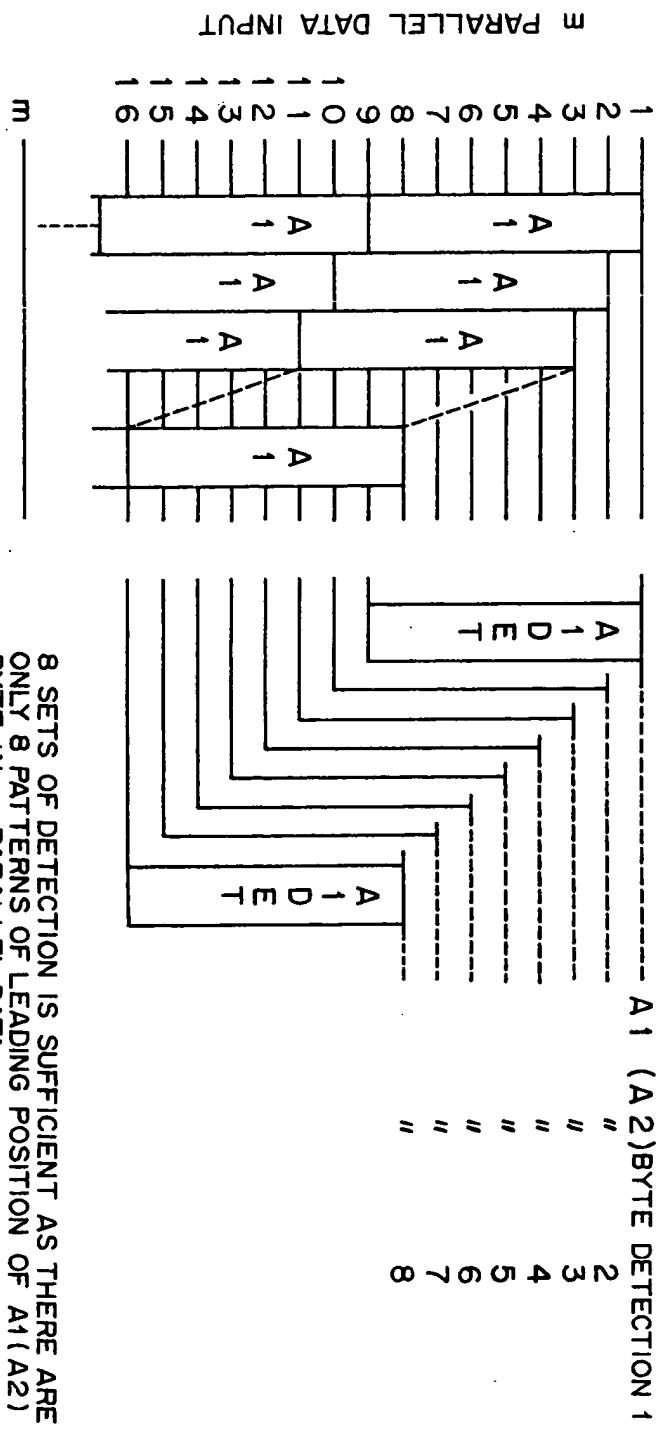
FIG. 7

- SUPPOSE THE ACTUAL FRAME PATTERN BE 4 BYTES AT INCLUDING A1/A2 BOUNDARY





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F I G. 9

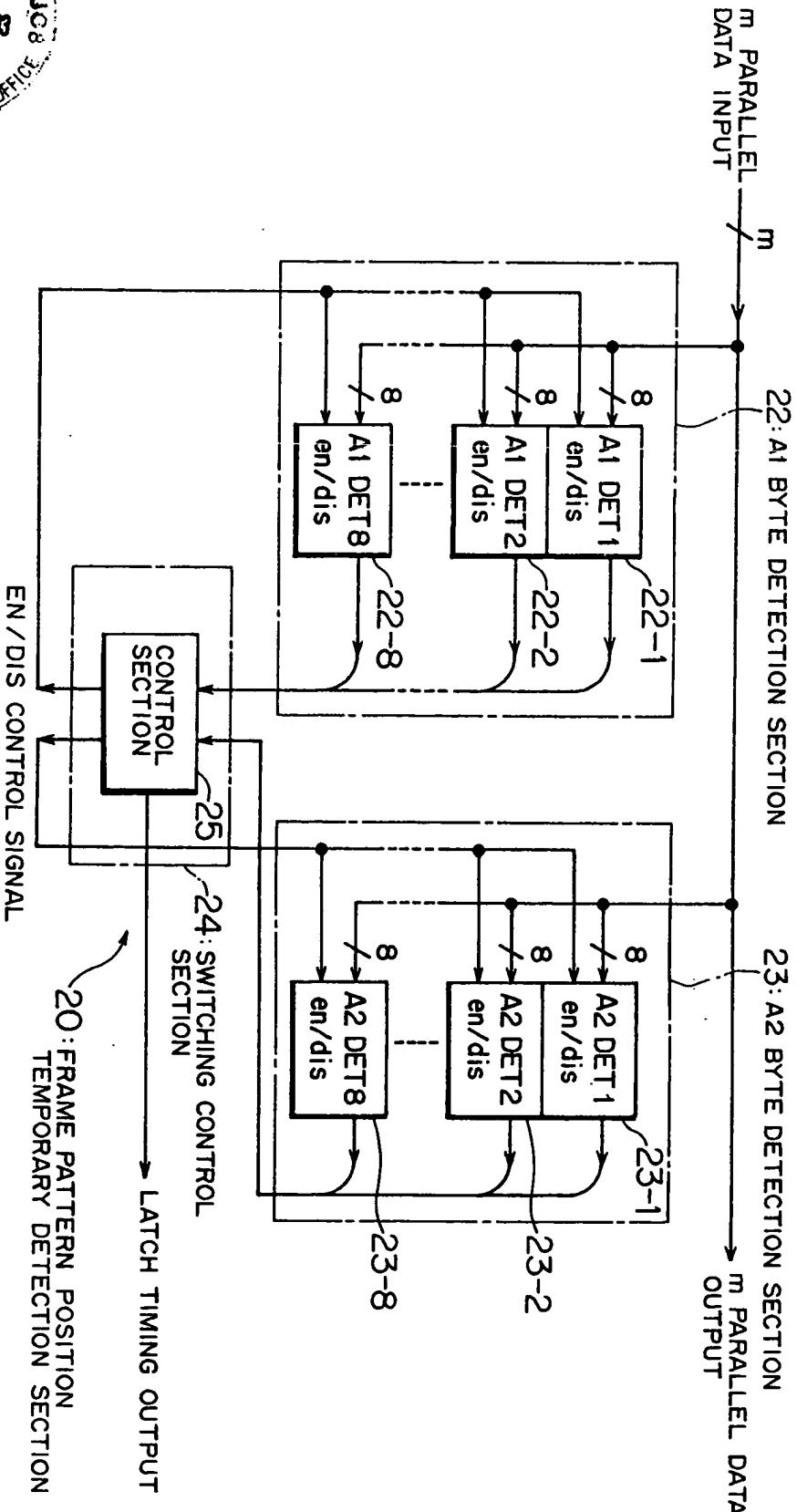


FIG. 10

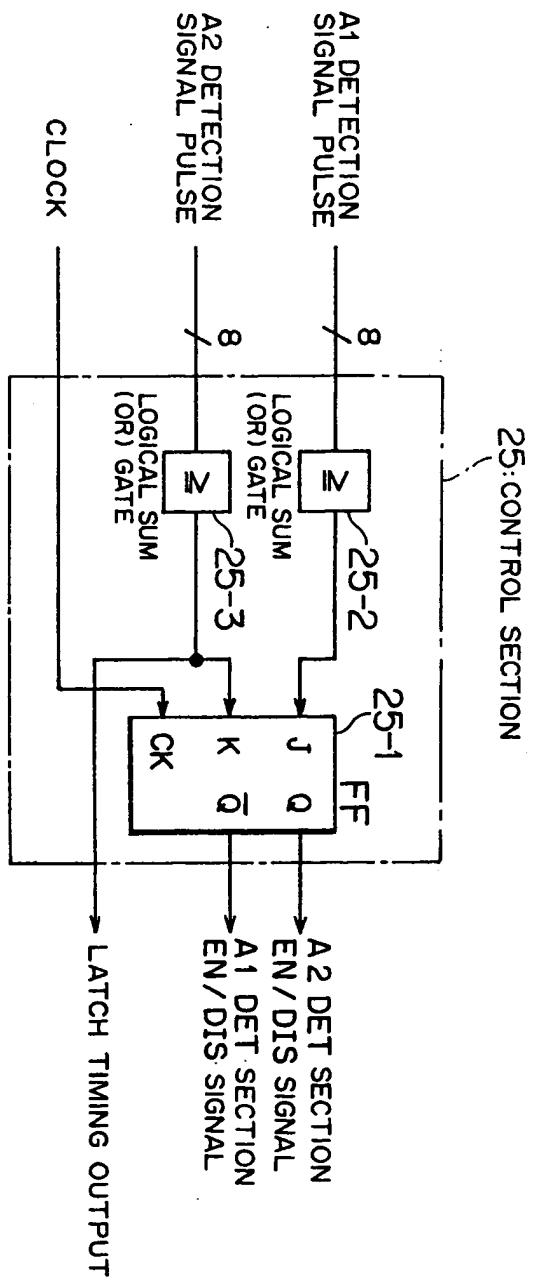




FIG. II

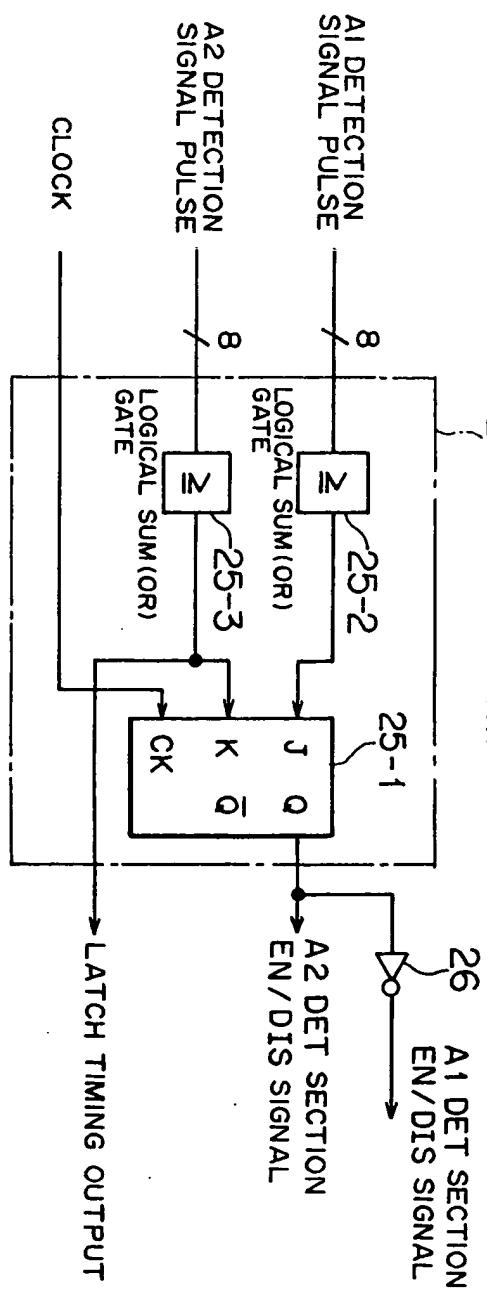




FIG. 12(a) <sub>m</sub> PARALLEL DATA

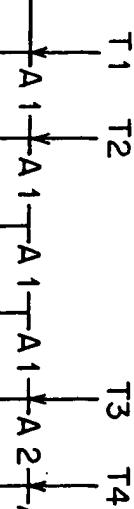


FIG. 12(b) A<sub>1</sub> DET

A<sub>2</sub> DET

FIG. 12(c) A<sub>2</sub> DET

FIG. 12(d) EN/DIS SIGNAL

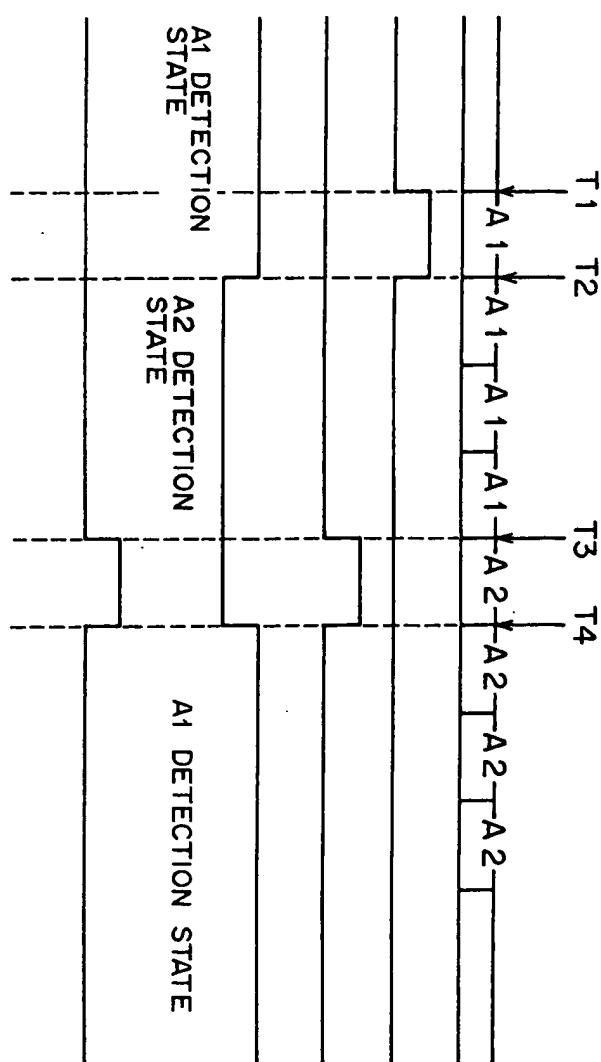


FIG. 12(e) LATCH TIMING



FIG. 13(a) CLOCK

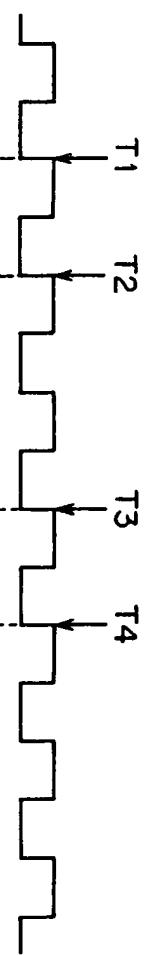


FIG. 13(b) A<sub>1</sub> DETECTION SIGNAL PULSE

FIG. 13(c) A<sub>2</sub> DETECTION SIGNAL PULSE

FIG. 13(d) A<sub>2</sub> DET SECTION EN/DIS SIGNAL

FIG. 13(e) LATCH TIMING

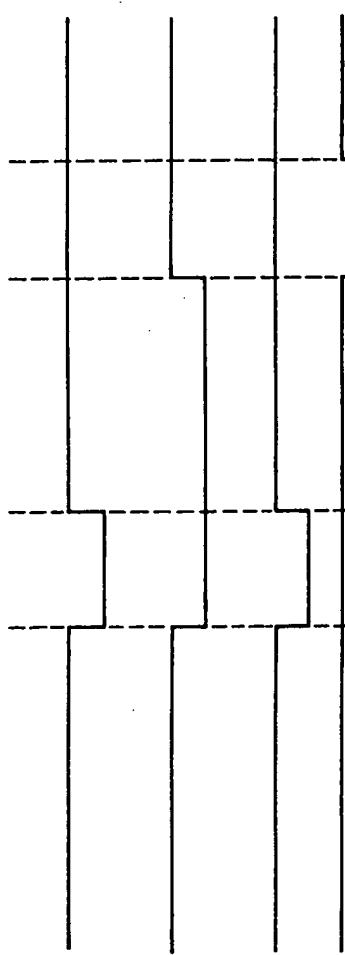


FIG. 14

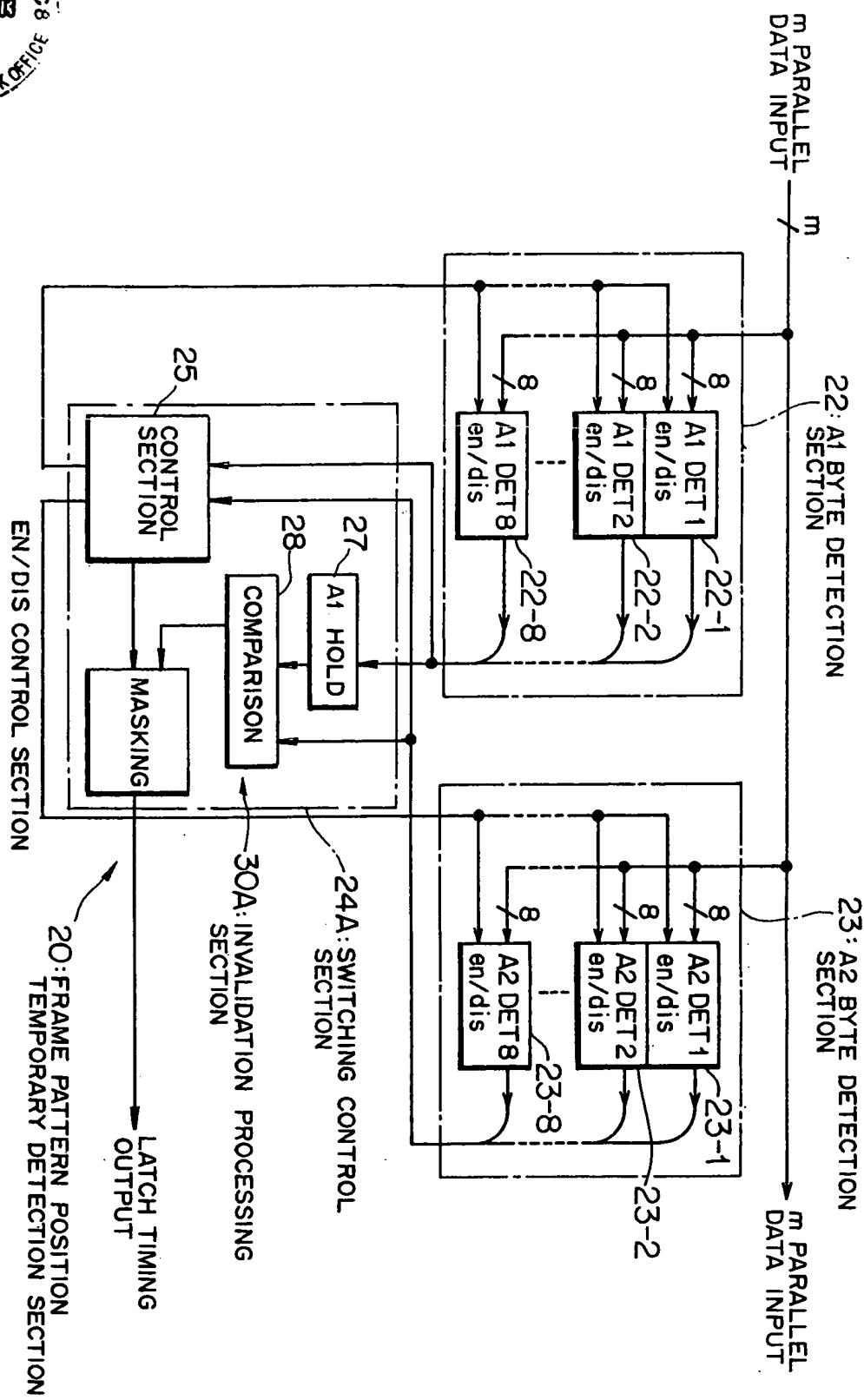
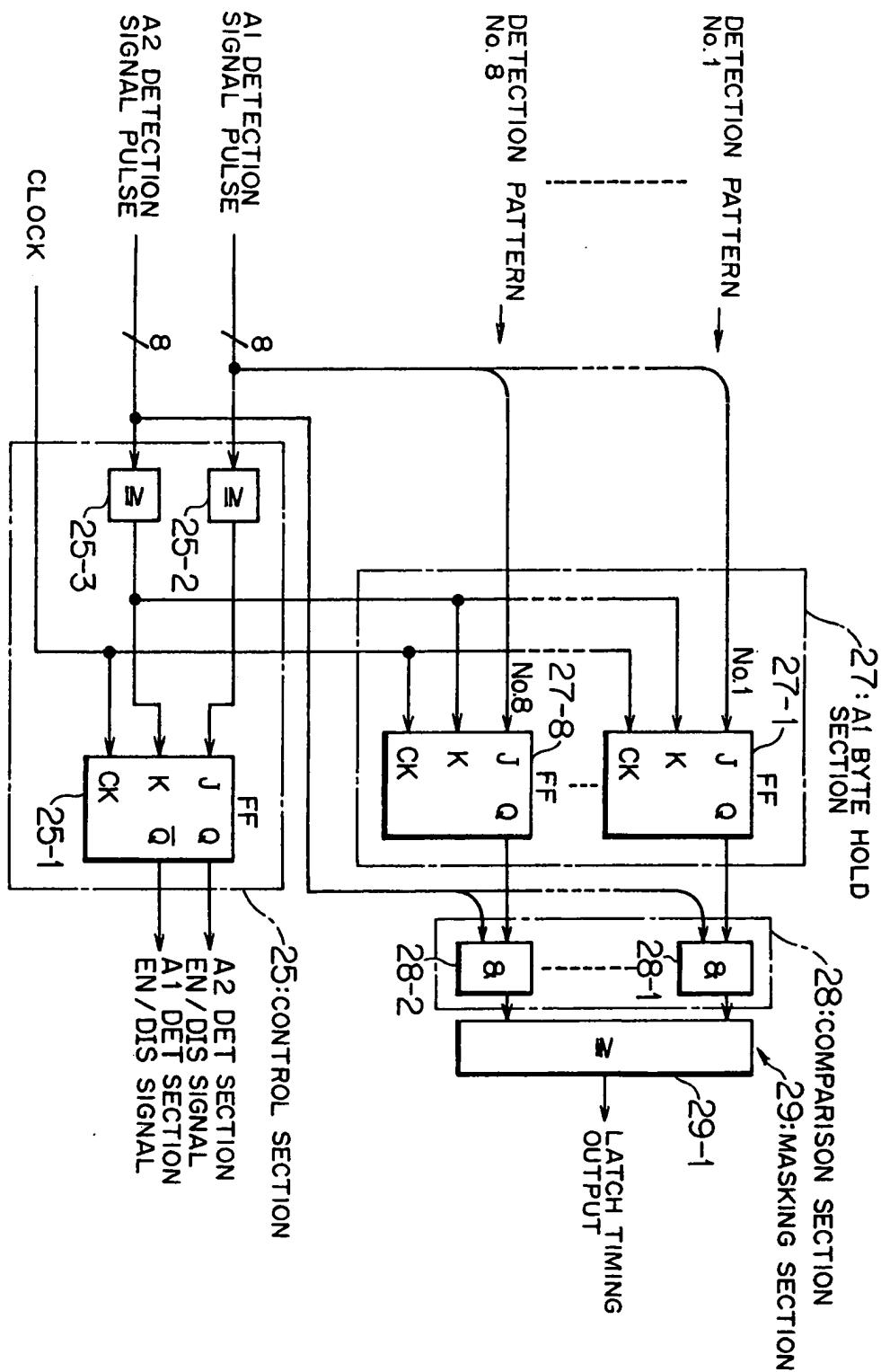


FIG. 15



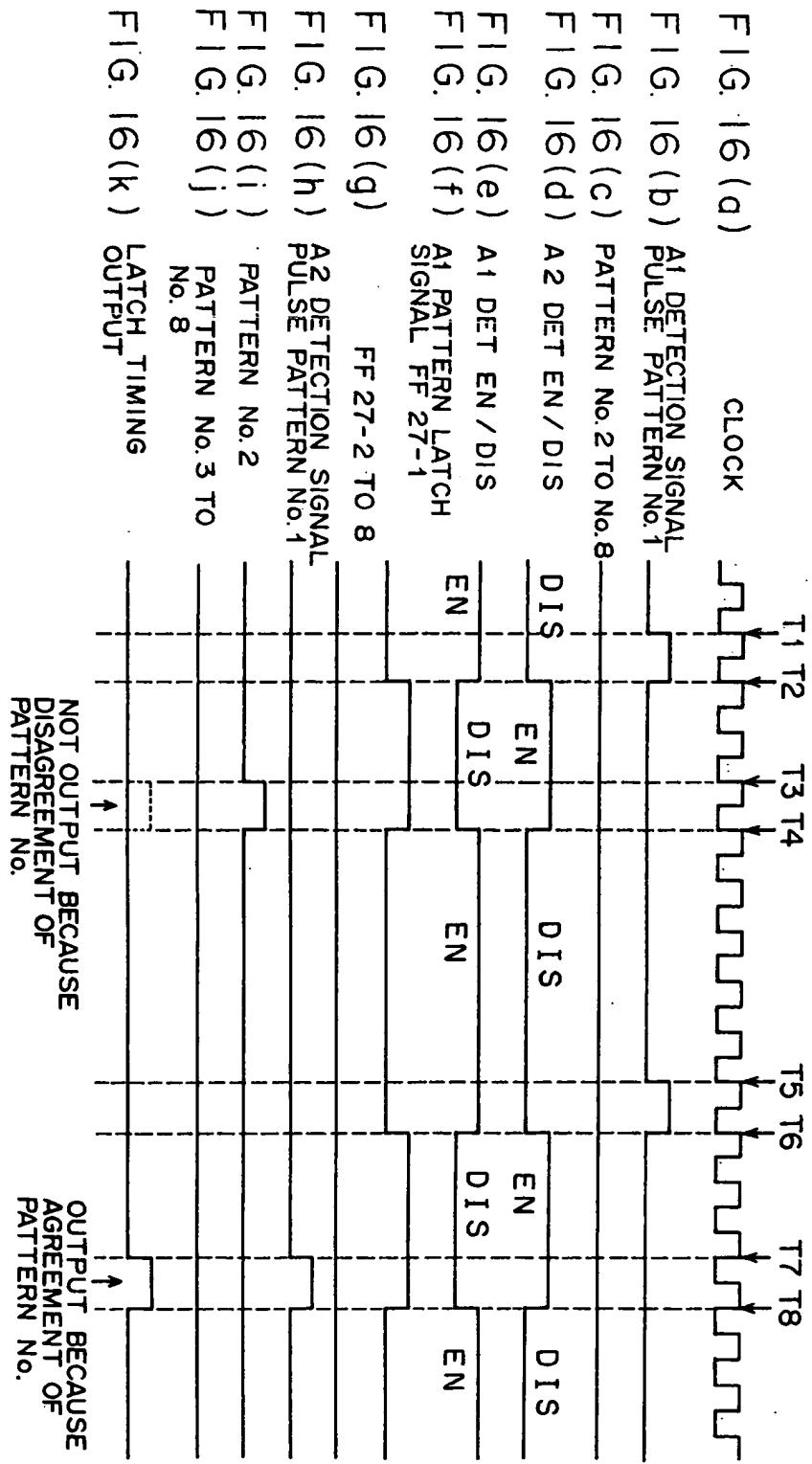


FIG. 17

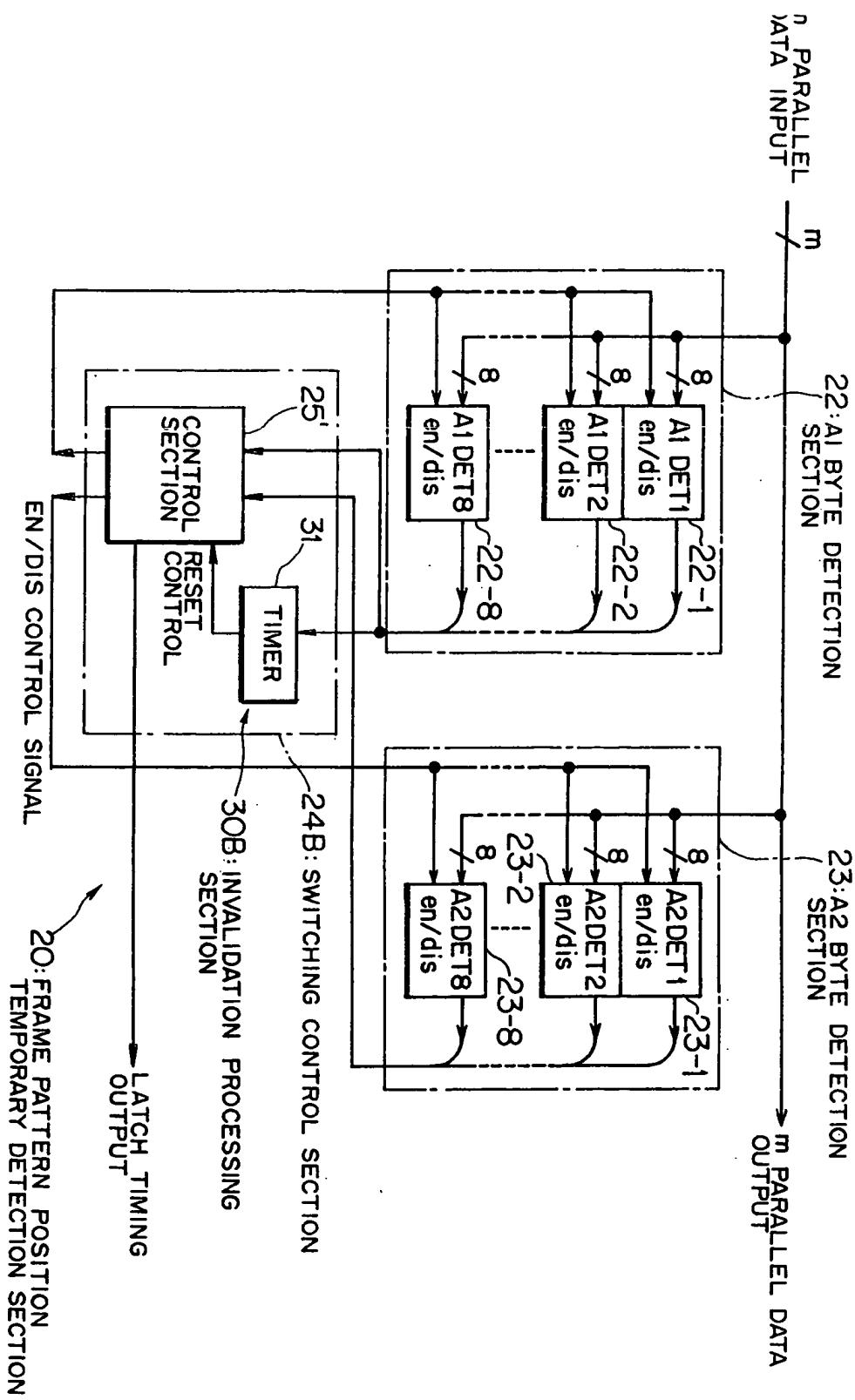


FIG. 18

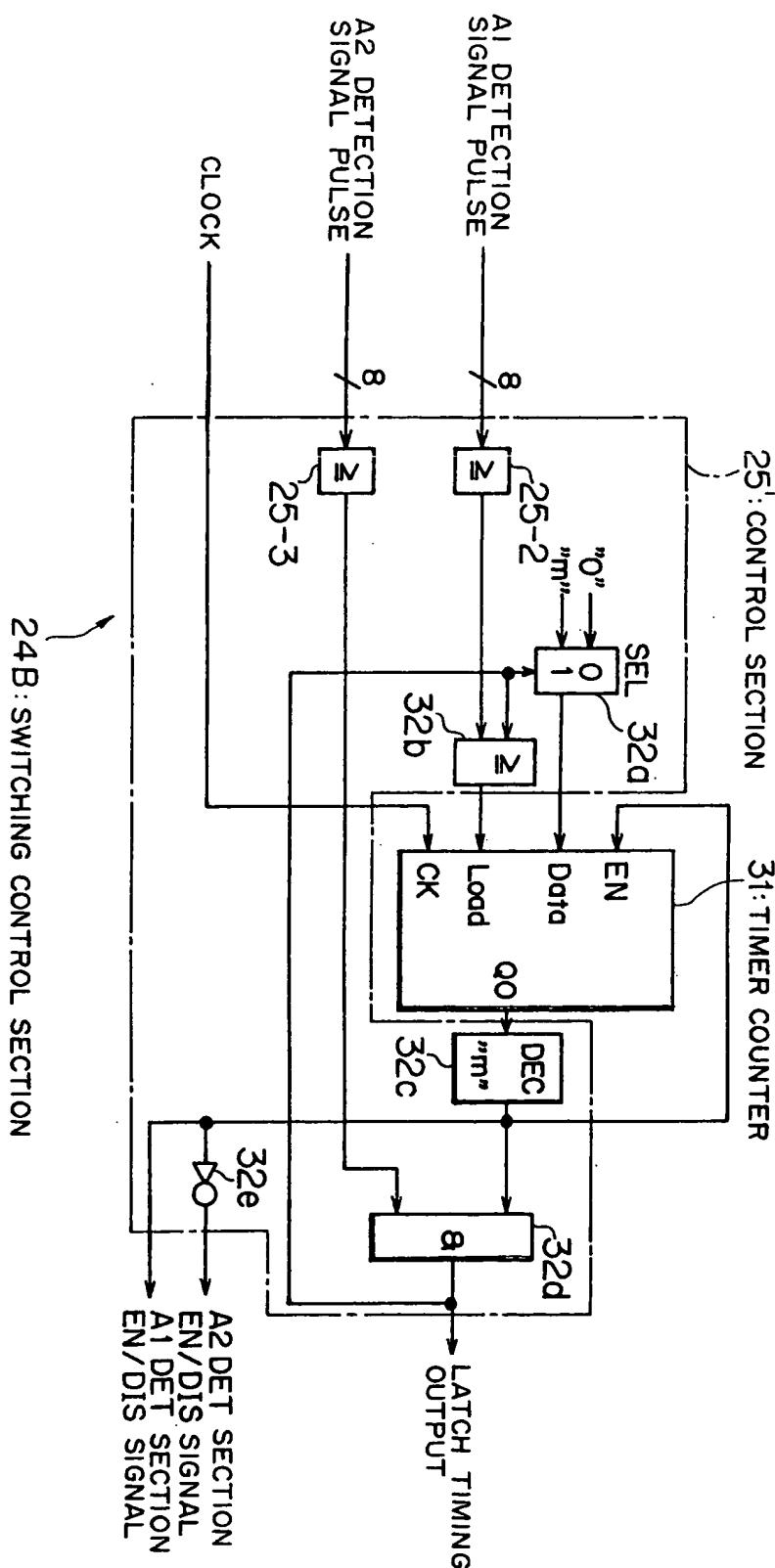


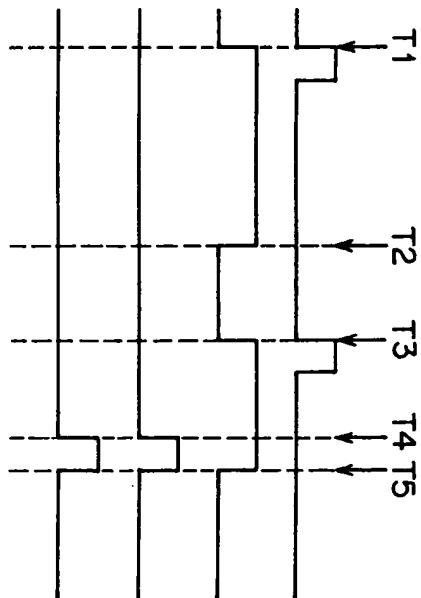


FIG. 19(a) LOAD INPUT

FIG. 19(b) Q OUTPUT

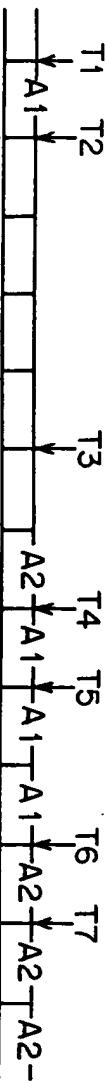
FIG. 19(c) A2 INPUT

FIG. 19(d) LATCH TIMING





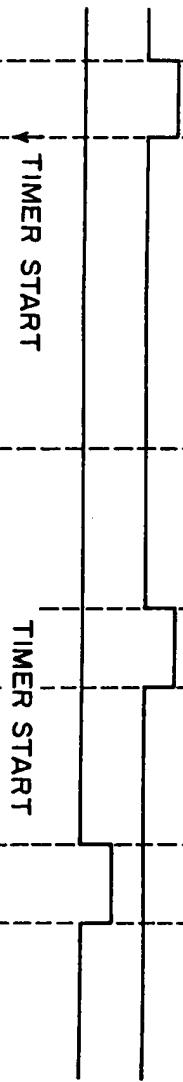
**FIG. 20(a)<sub>m</sub> PARALLEL DATA**



**FIG. 20(b)  
FIG. 20(c)**

A<sub>1</sub> DET  
A<sub>2</sub> DET

**FIG. 20(d) TIMER OUTPUT**



**FIG. 20(e)<sup>EN/DIS SIGNAL</sup>**

A<sub>1</sub> DETECTION  
STATE

A<sub>2</sub> DETECTION  
STATE

A<sub>1</sub> DETECTION  
STATE

A<sub>2</sub> DETECTION  
STATE

**FIG. 20(f) LATCH TIMING OUTPUT**

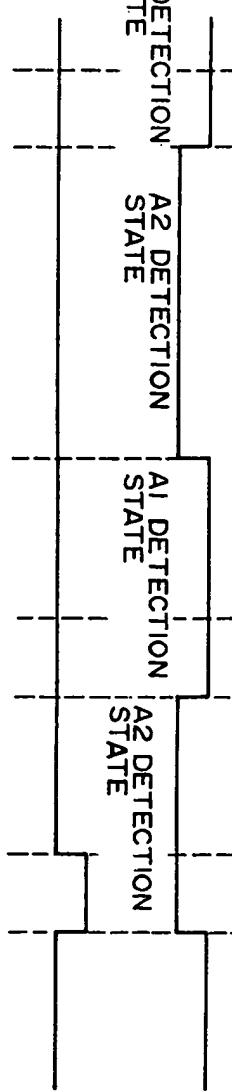


FIG. 2

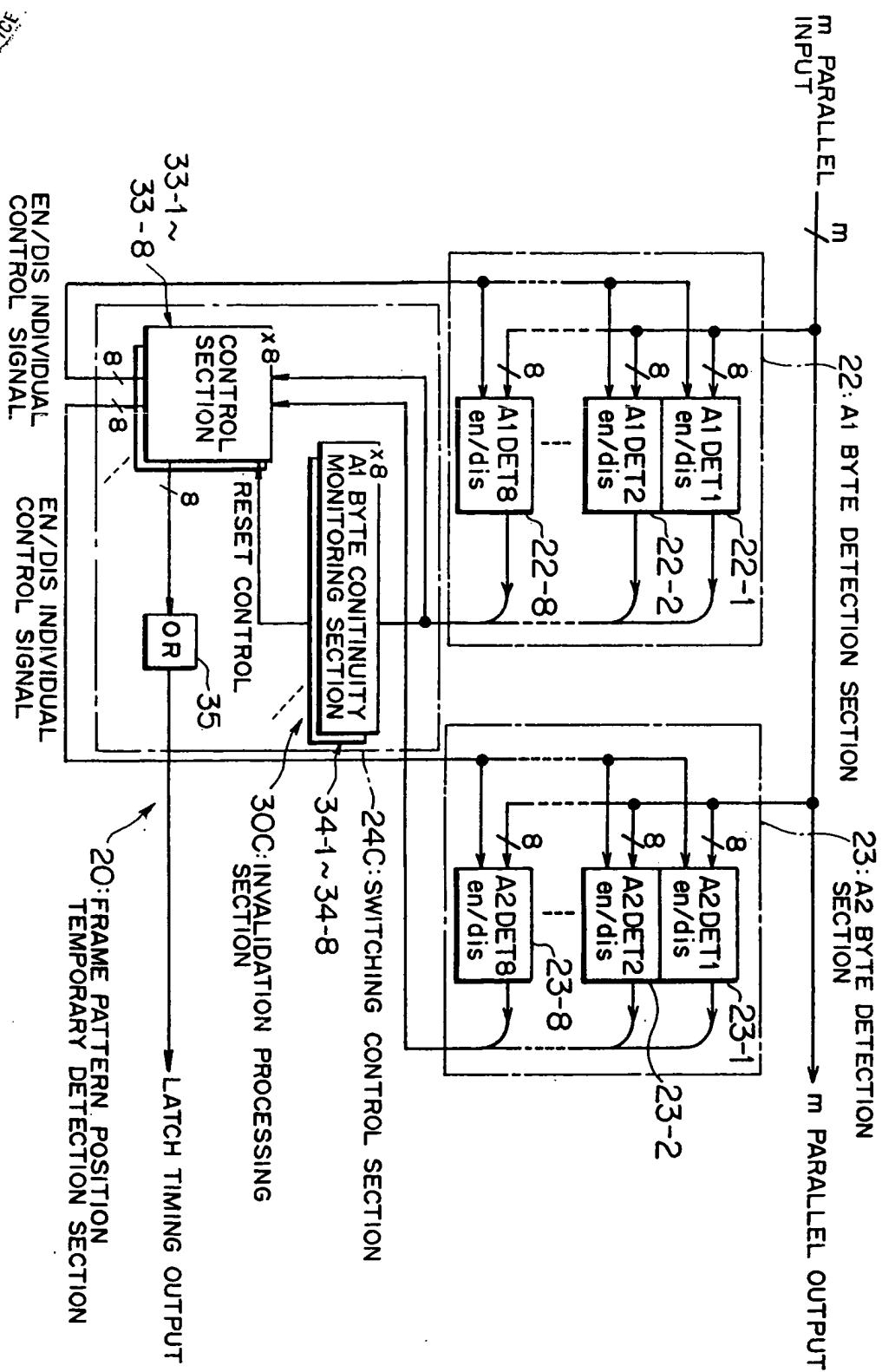


FIG. 22

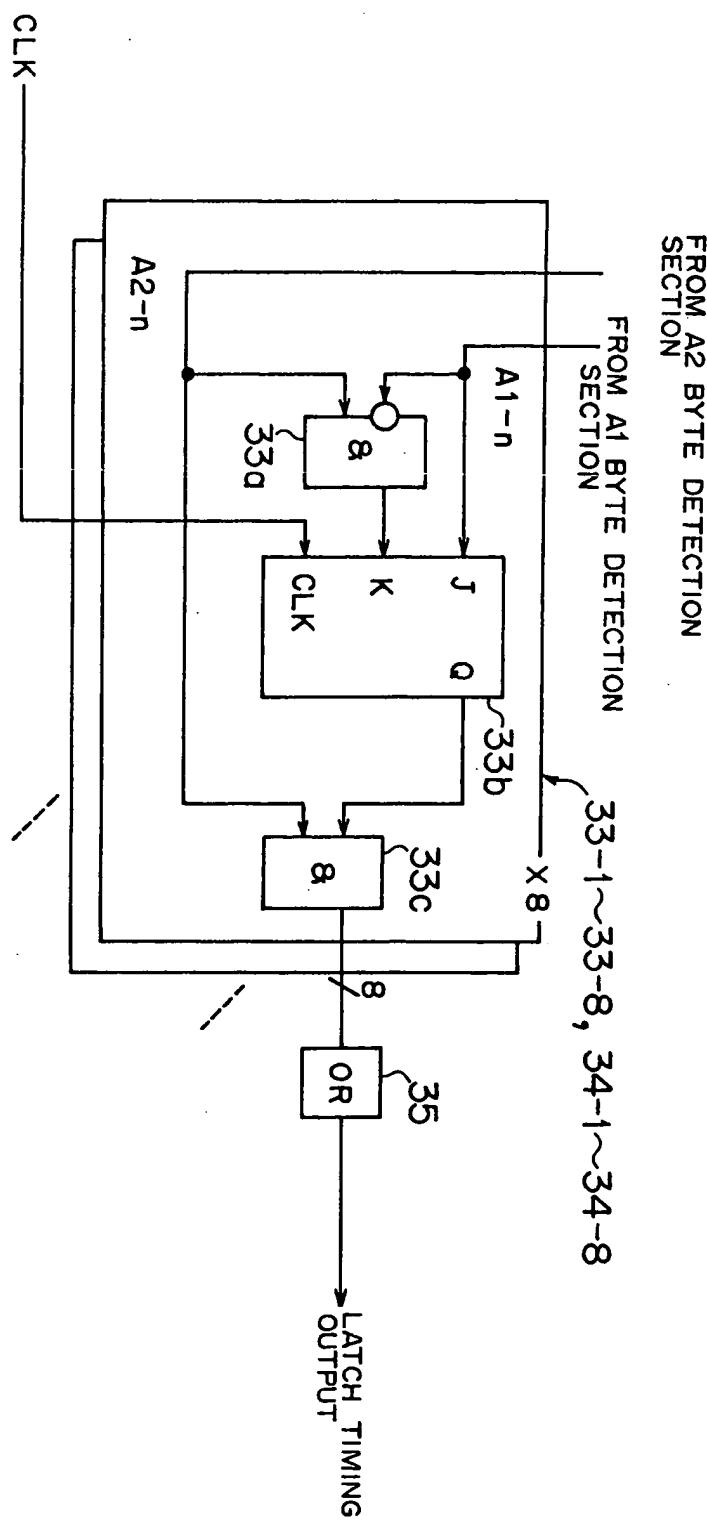




FIG. 23 (a) m PARALLEL DATA

FIG. 23 (b)

FIG. 23 (c)

FIG. 23 (d)

A1 DET  
A2 DET  
EN/DIS CONTROL

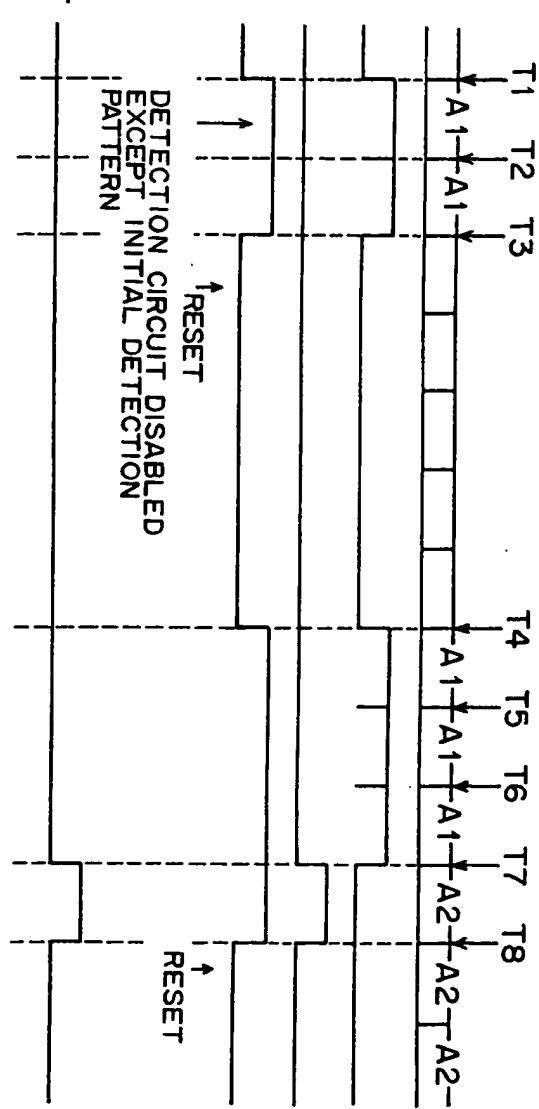


FIG. 23 (e) LATCH TIMING OUTPUT

FIG. 24

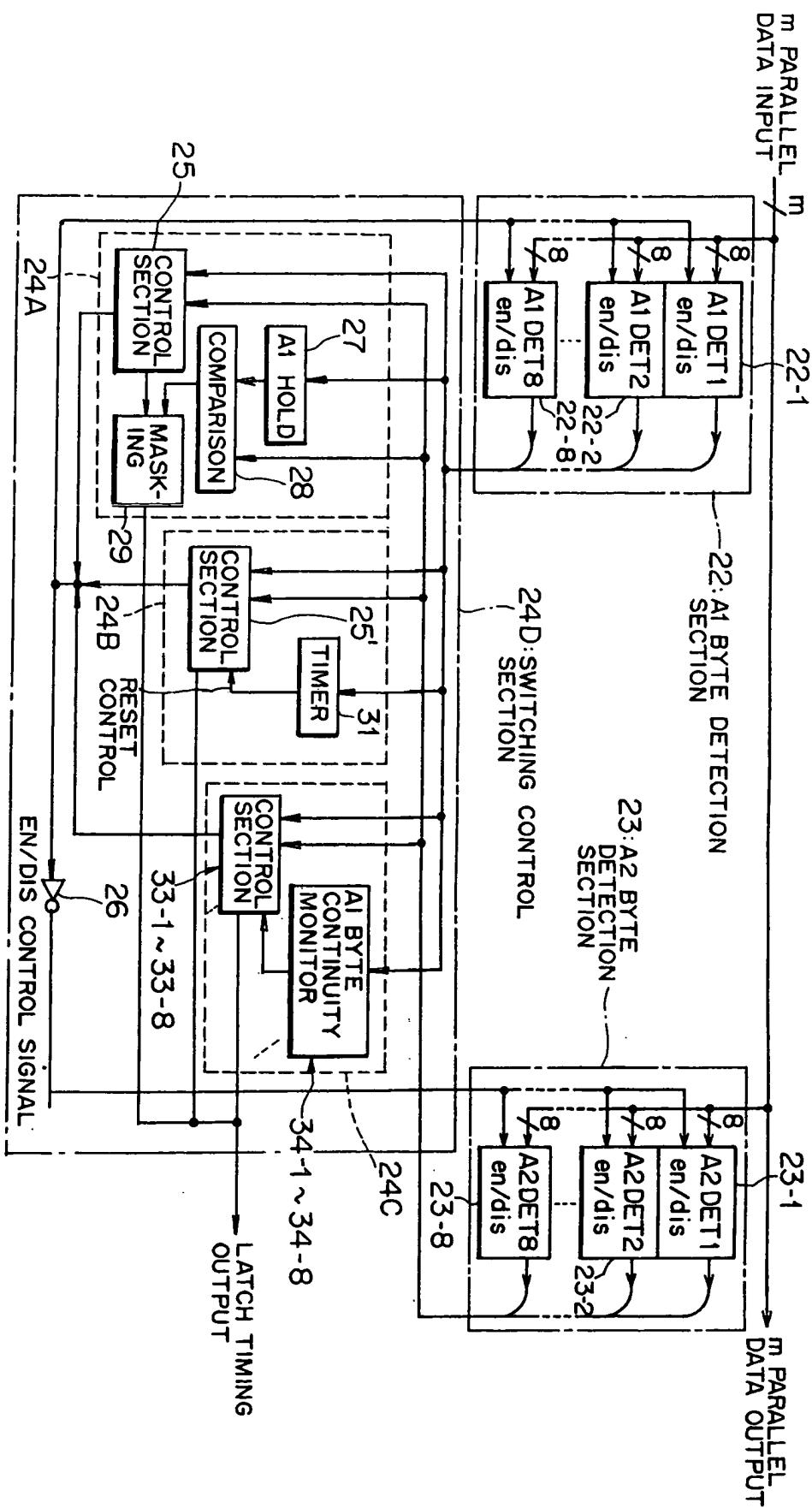


FIG.25

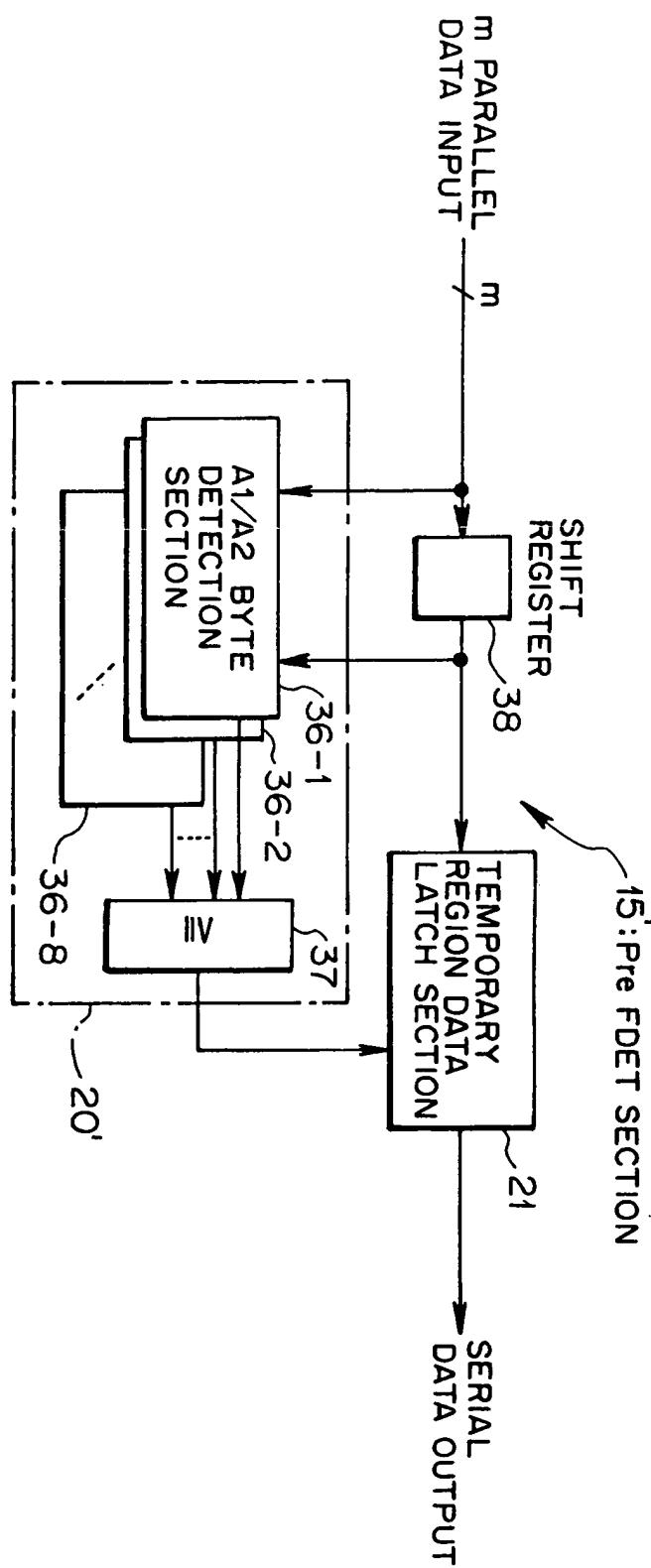


FIG.26

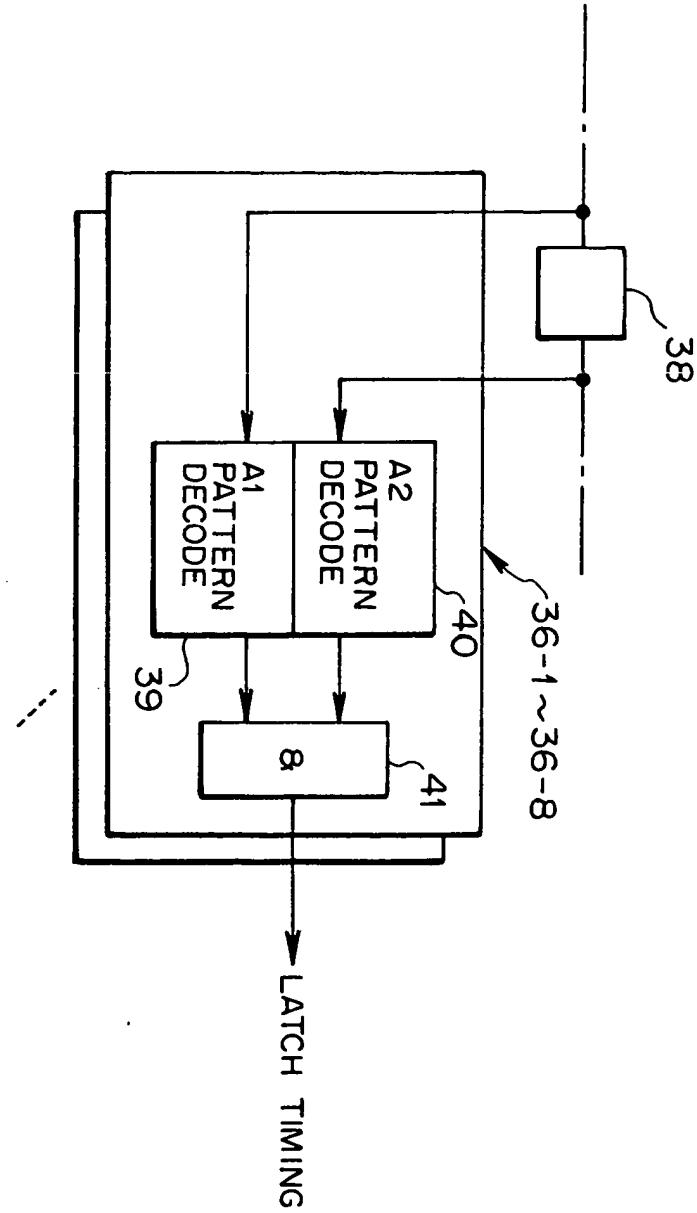
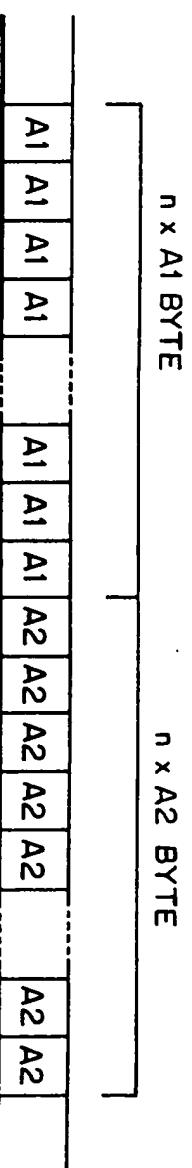




FIG. 27(a) SERIAL DATA



↓ m PARALLELIZATION (IF m = 16)

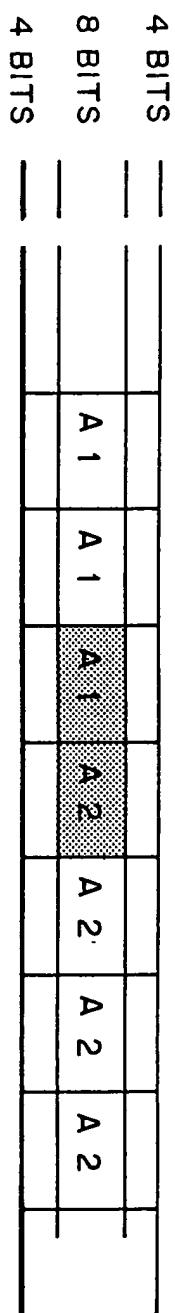
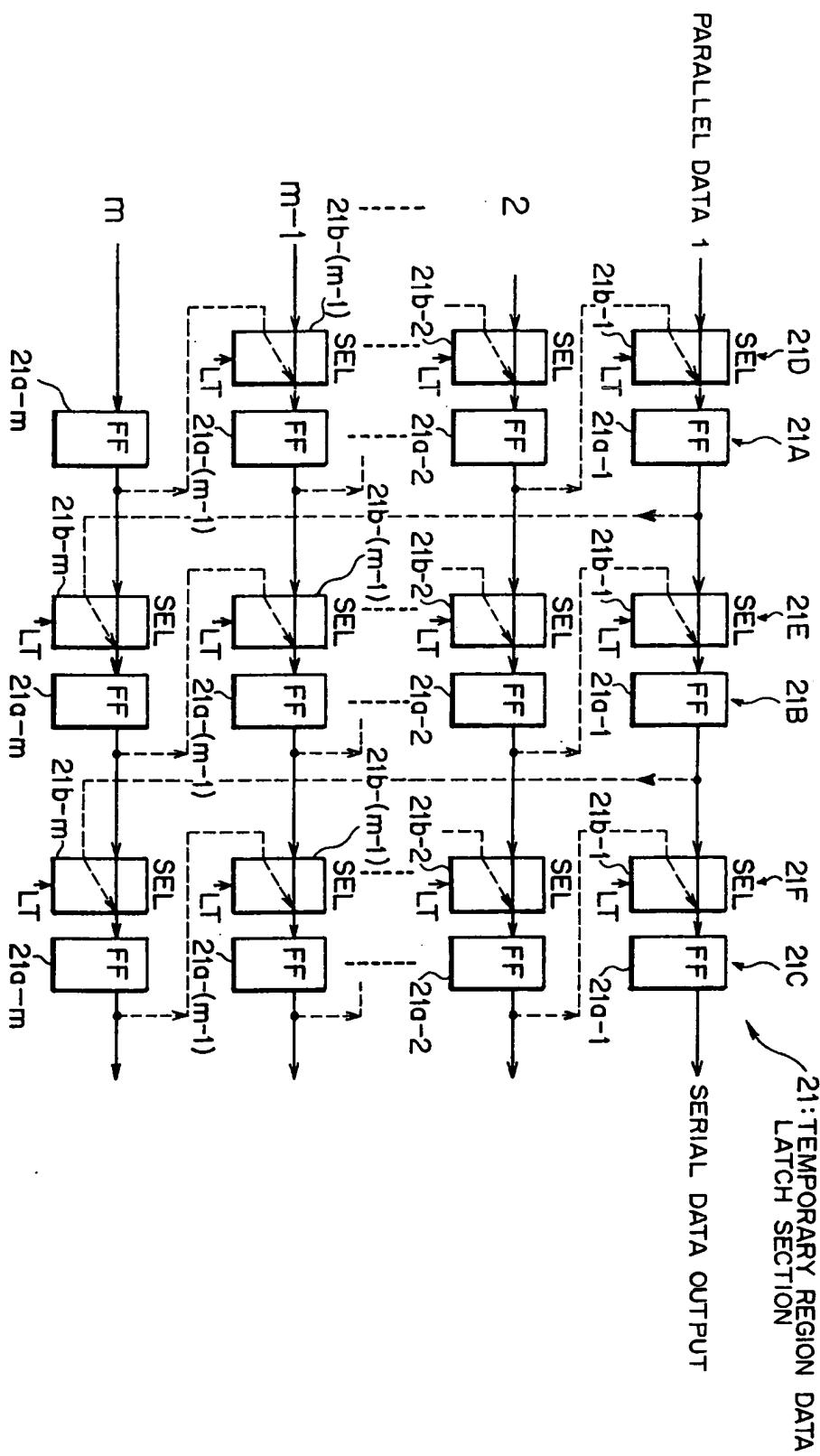


FIG. 27(b)

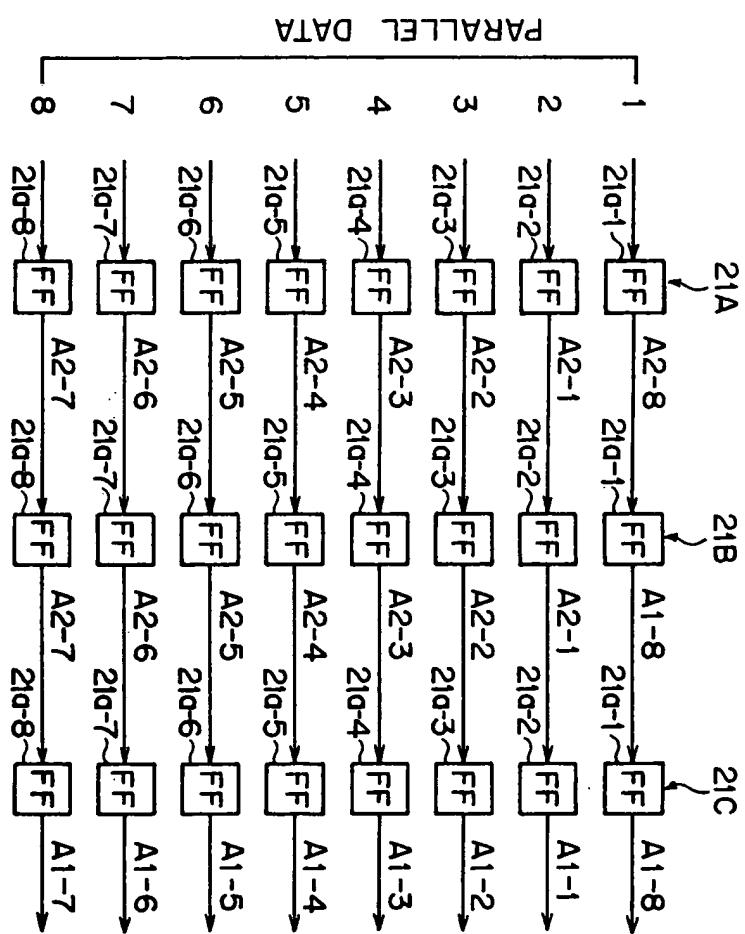


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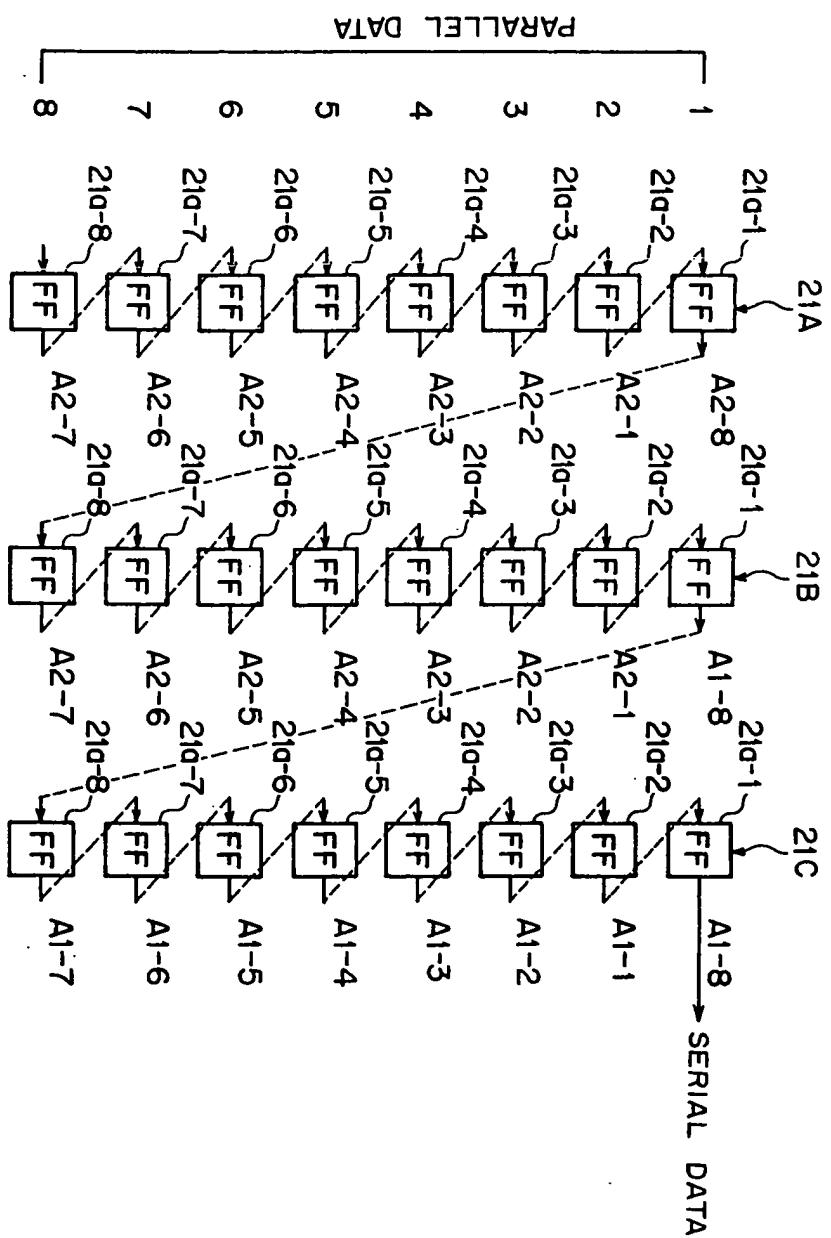


LT:LATCH TIMING SIGNAL

FIG. 29



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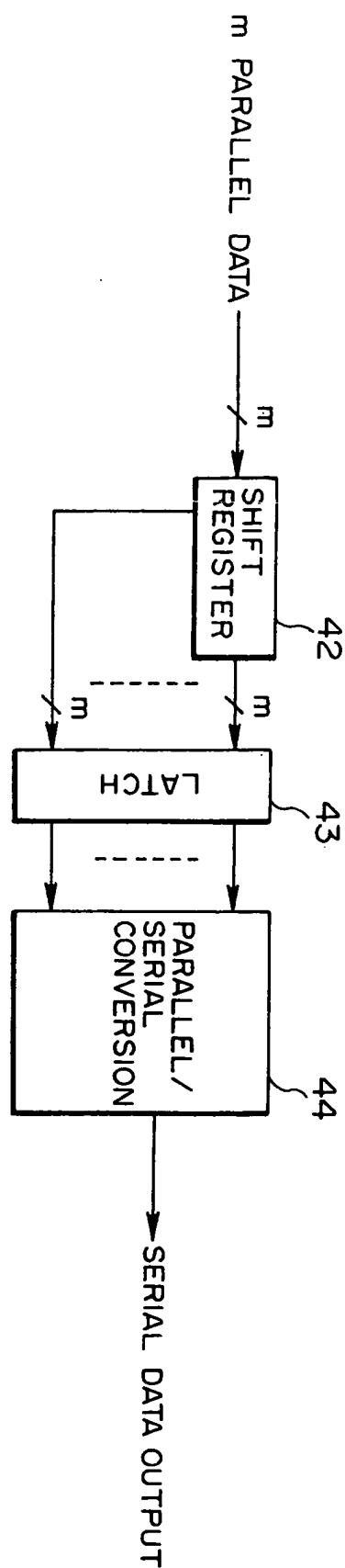


FIG. 31

FIG.32

14: FRAME SYNCHRONOUS PATTERN  
DETECTION APPARATUS

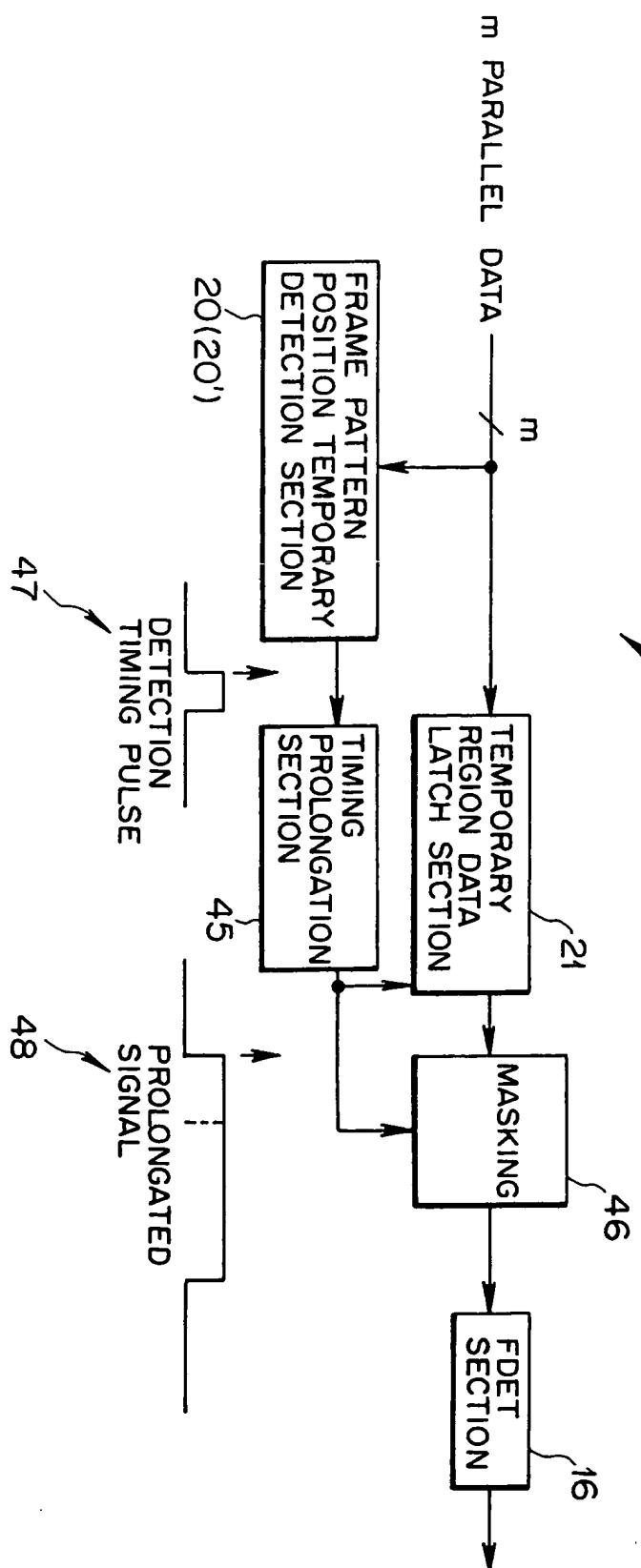


FIG. 33

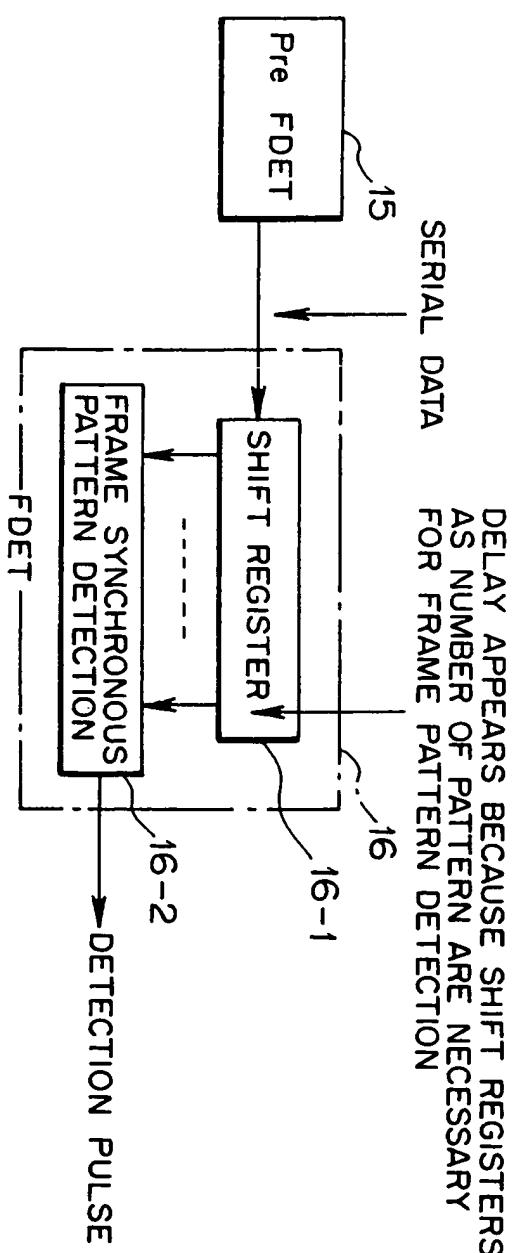




FIG. 34

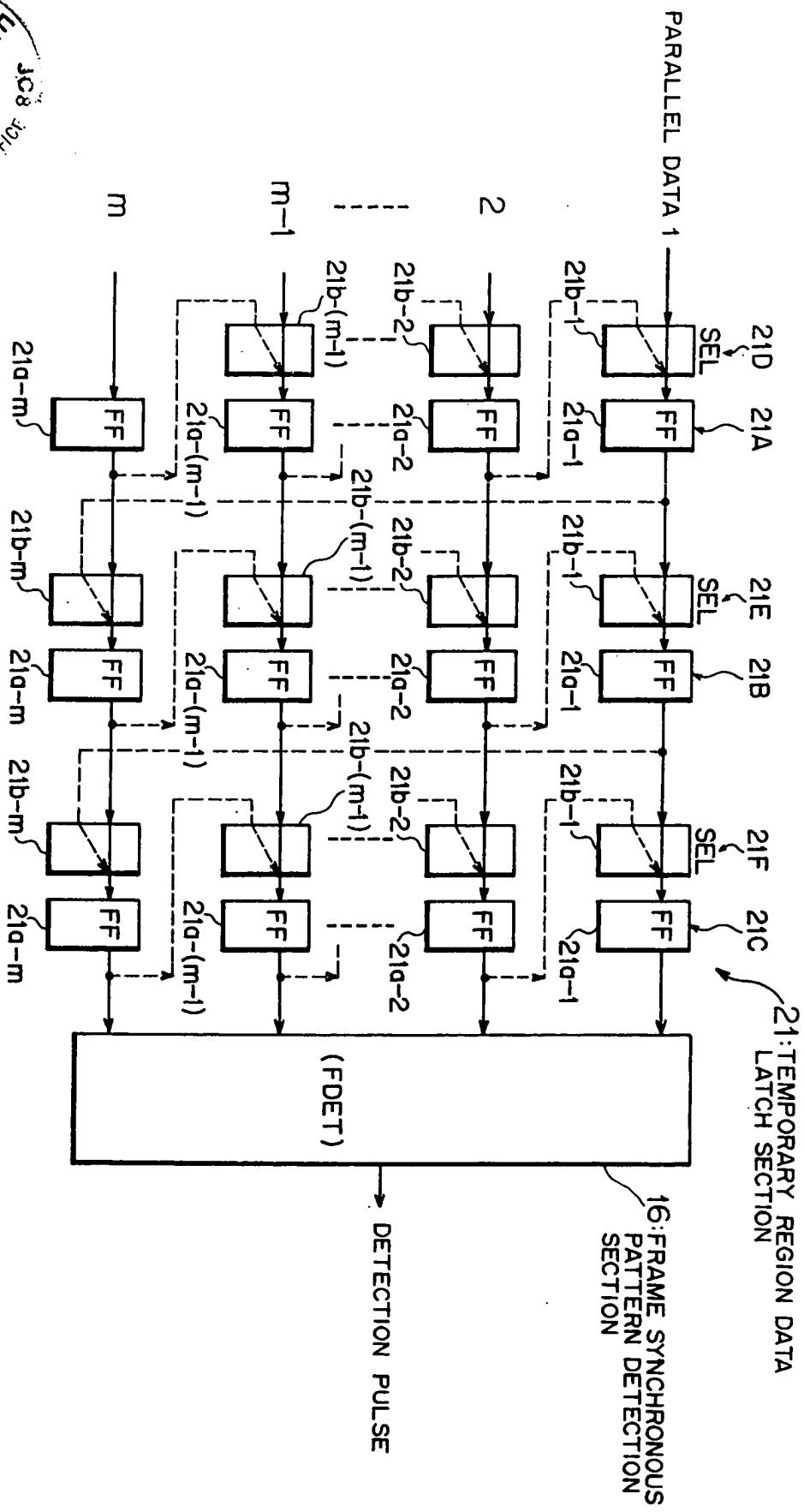




FIG. 35

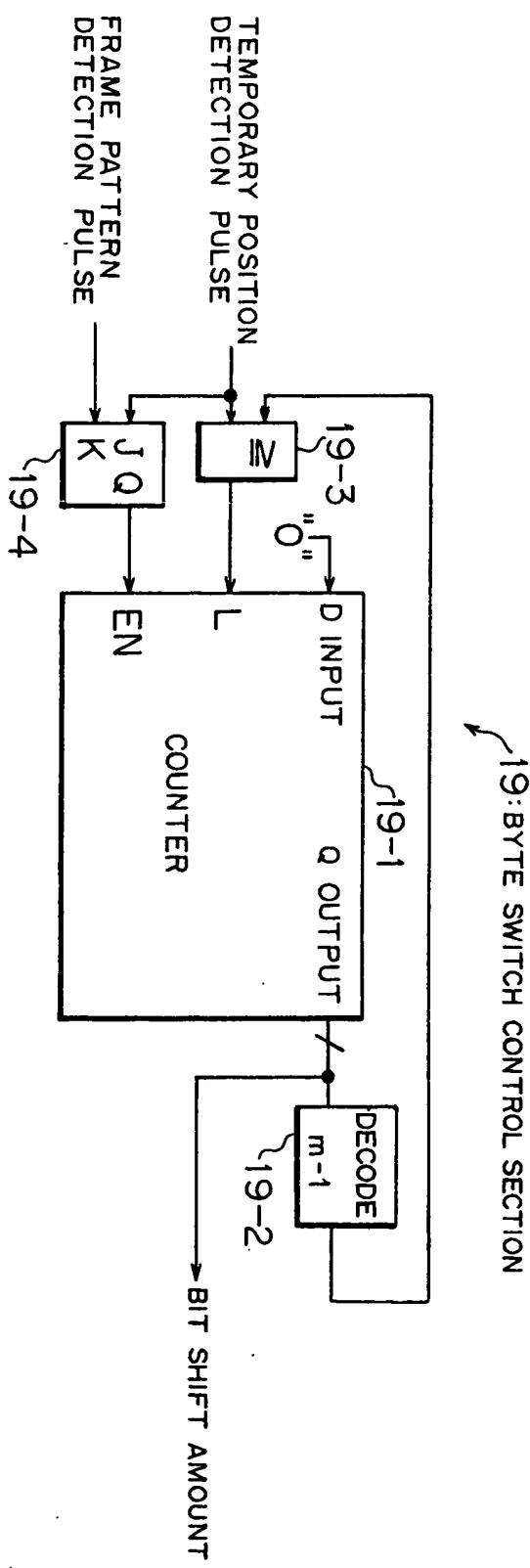




FIG. 36(a)

PRE FDET OUTPUT  
TEMPORARY  
POSITION DETECTION  
PULSE

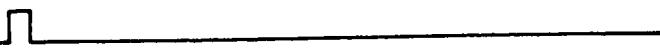


FIG. 36(b)

FDET OUTPUT  
FRAME PATTERN  
DETECTION PULSE

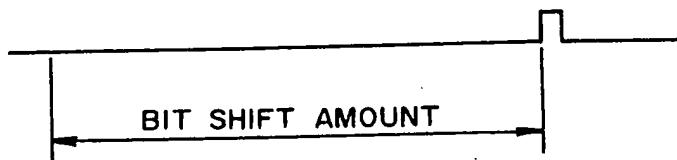


FIG. 37

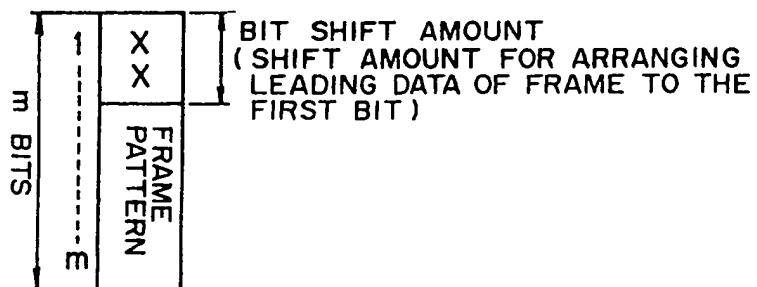




FIG. 38

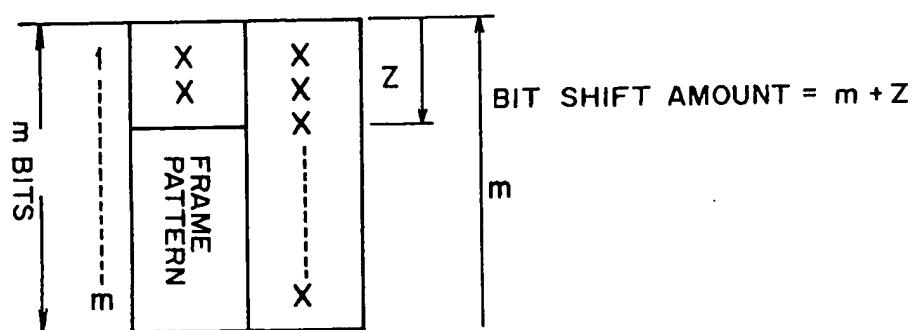




FIG. 39(a) TEMPORARY POSITION DETECTION PULSE

**FIG. 39(b)** FRAME PATTERN DETECTION PULSE  
**FIG. 39(c)** COUNTER EN (ENAEE)

FIG. 39(c) COUNTER EN (ENABLE)

## COUNTER OPERATION

**FIG. 39(d)** COUNTER L (LOAD)  
**FIG. 39(e)** COUNTER L VALUE

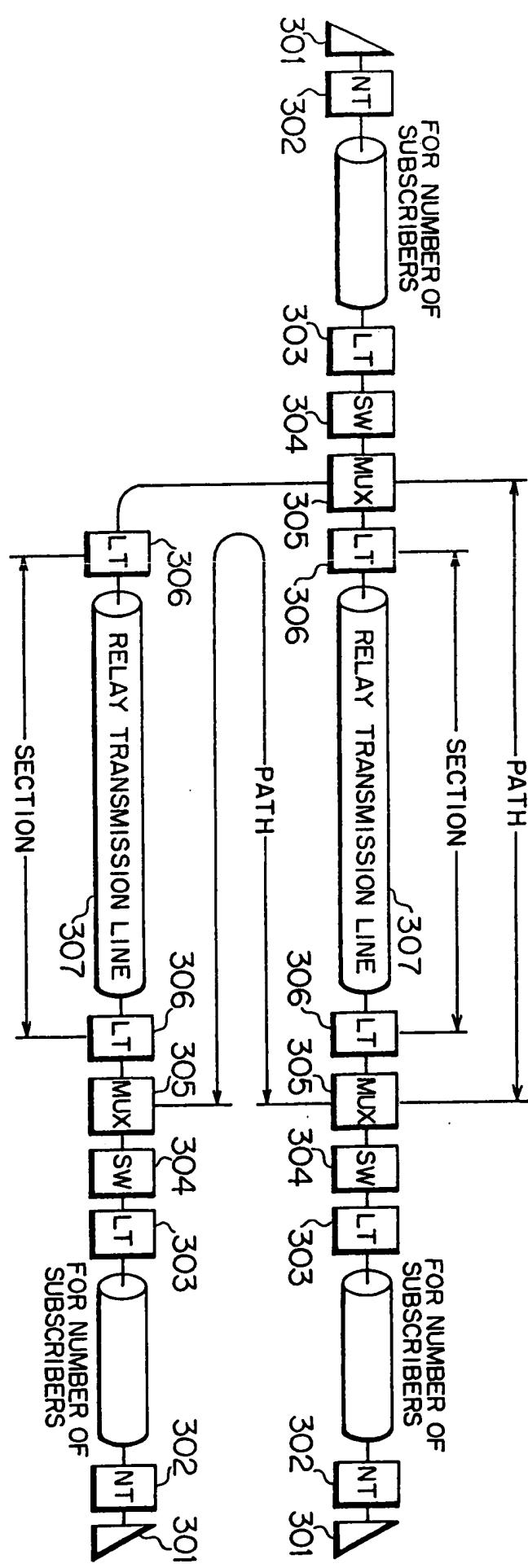
FIG. 39(e) COUNTER L VALUE

The diagram illustrates the timing sequence for counter operation. It features four signals:  $J$ ,  $K$ ,  $T_1$ , and  $T_2$ . The sequence is divided into two main sections by a dashed line labeled "COUNTER OPERATION".

- Top Section (Right of the dashed line):** This section shows the signals  $T_1$ ,  $T_2$ ,  $T_3$ , and  $T_4$ . The width of the pulse for  $T_1$  is labeled  $m$ .
- Bottom Section (Left of the dashed line):** This section shows the signals  $J$ ,  $K$ ,  $T_1$ , and  $T_2$ . The width of the pulse for  $J$  is labeled  $m$ , and the width of the pulse for  $K$  is labeled  $z$ .

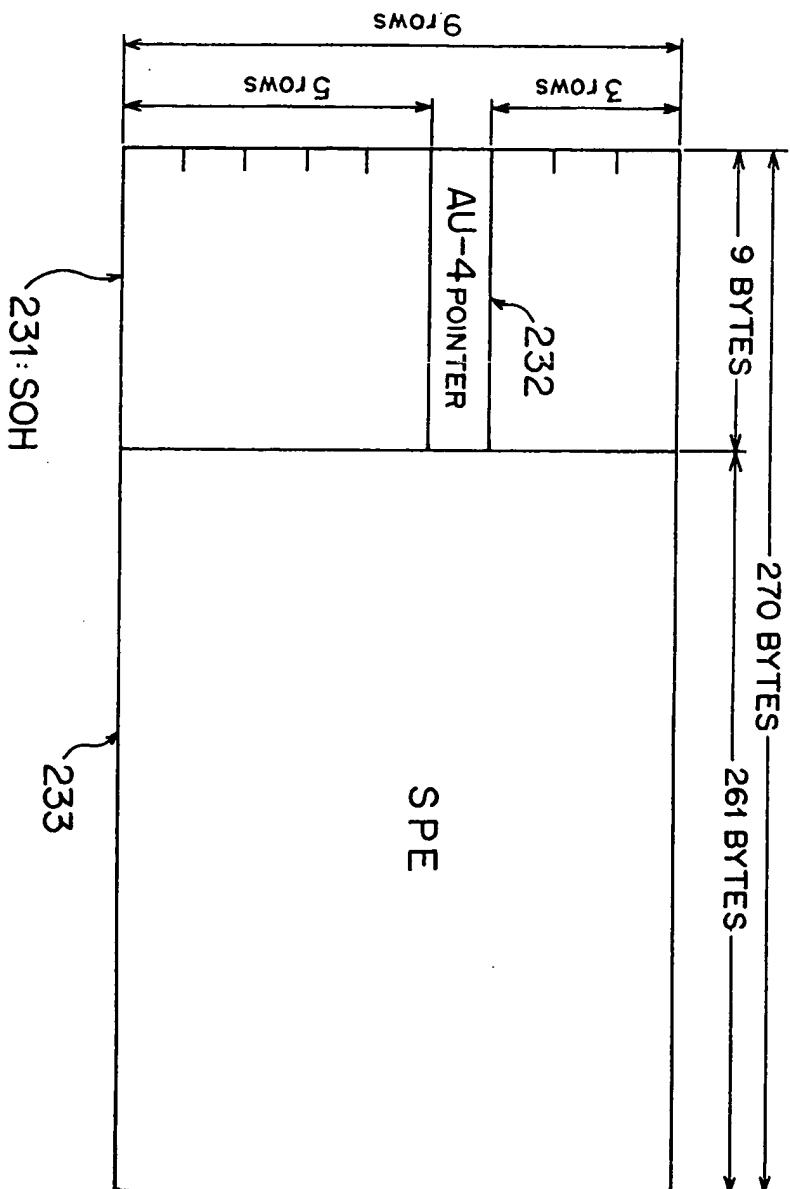


# FIG. 40

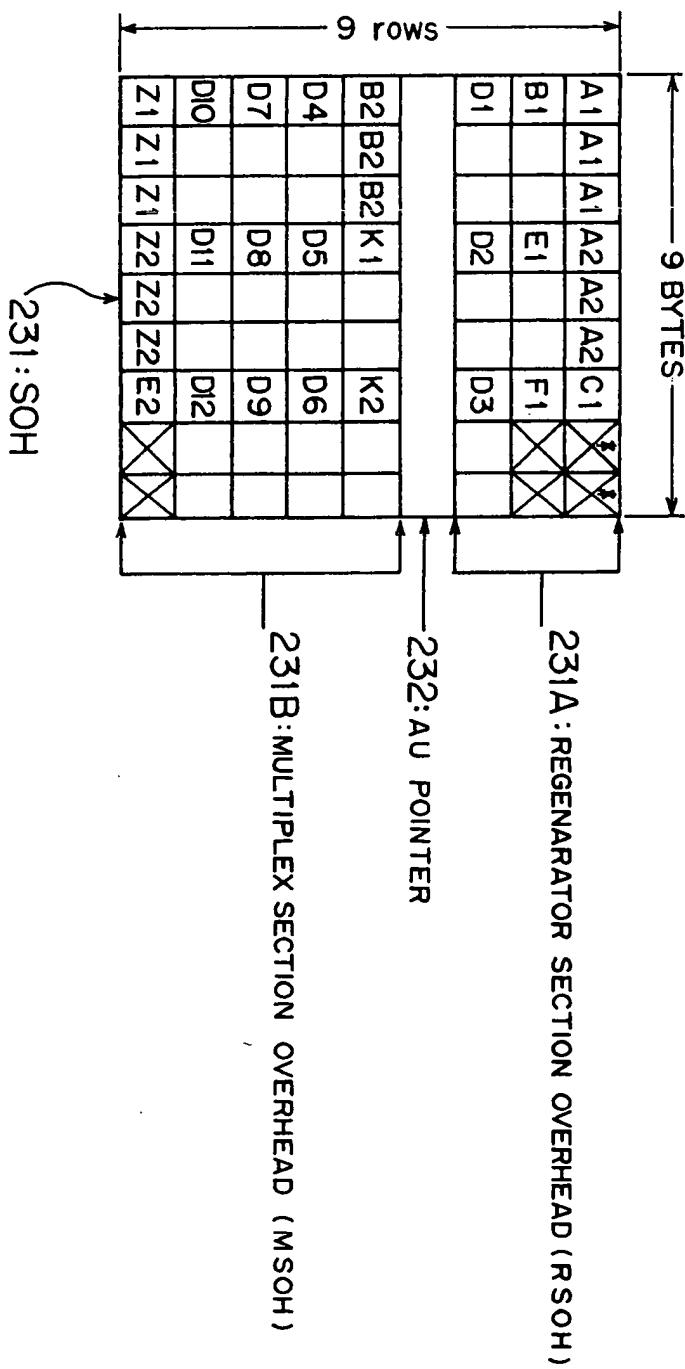




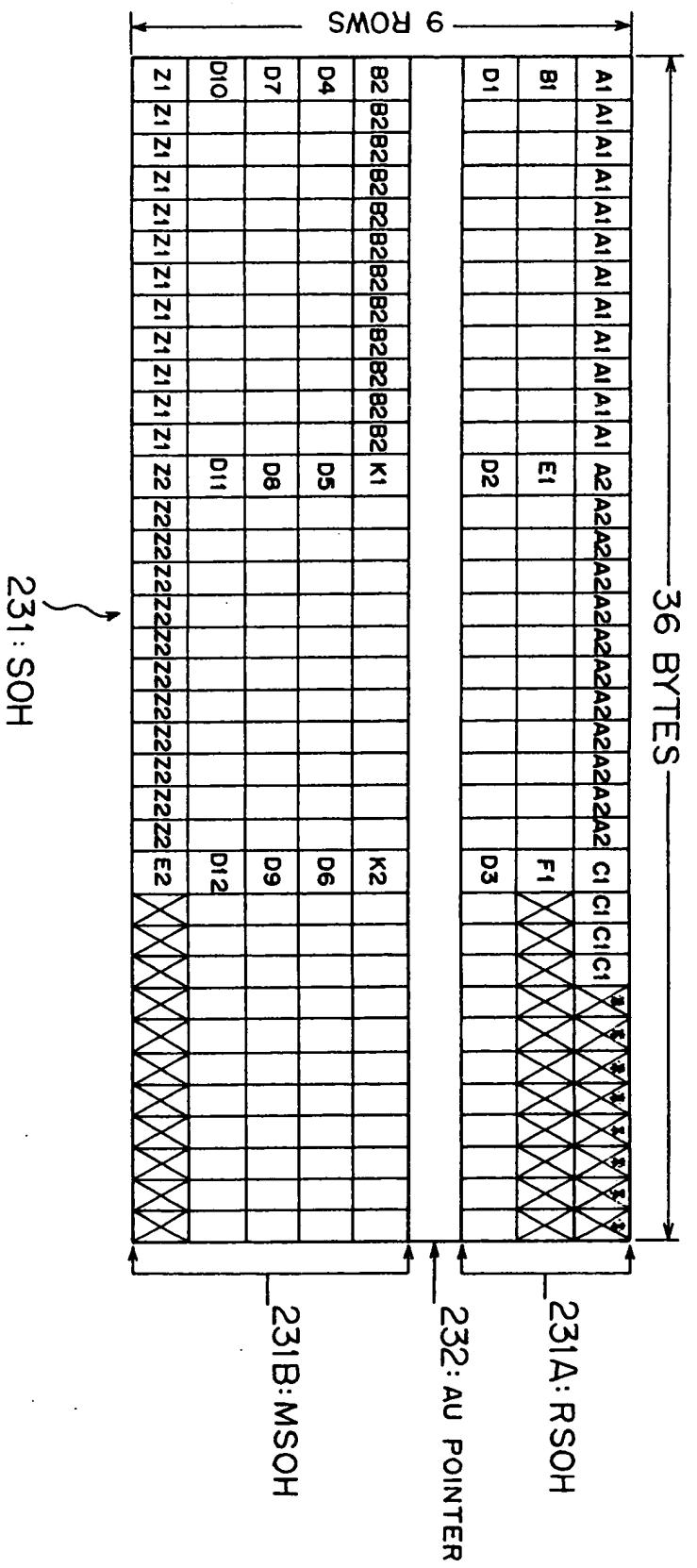
**FIG. 4I**  
PRIOR ART



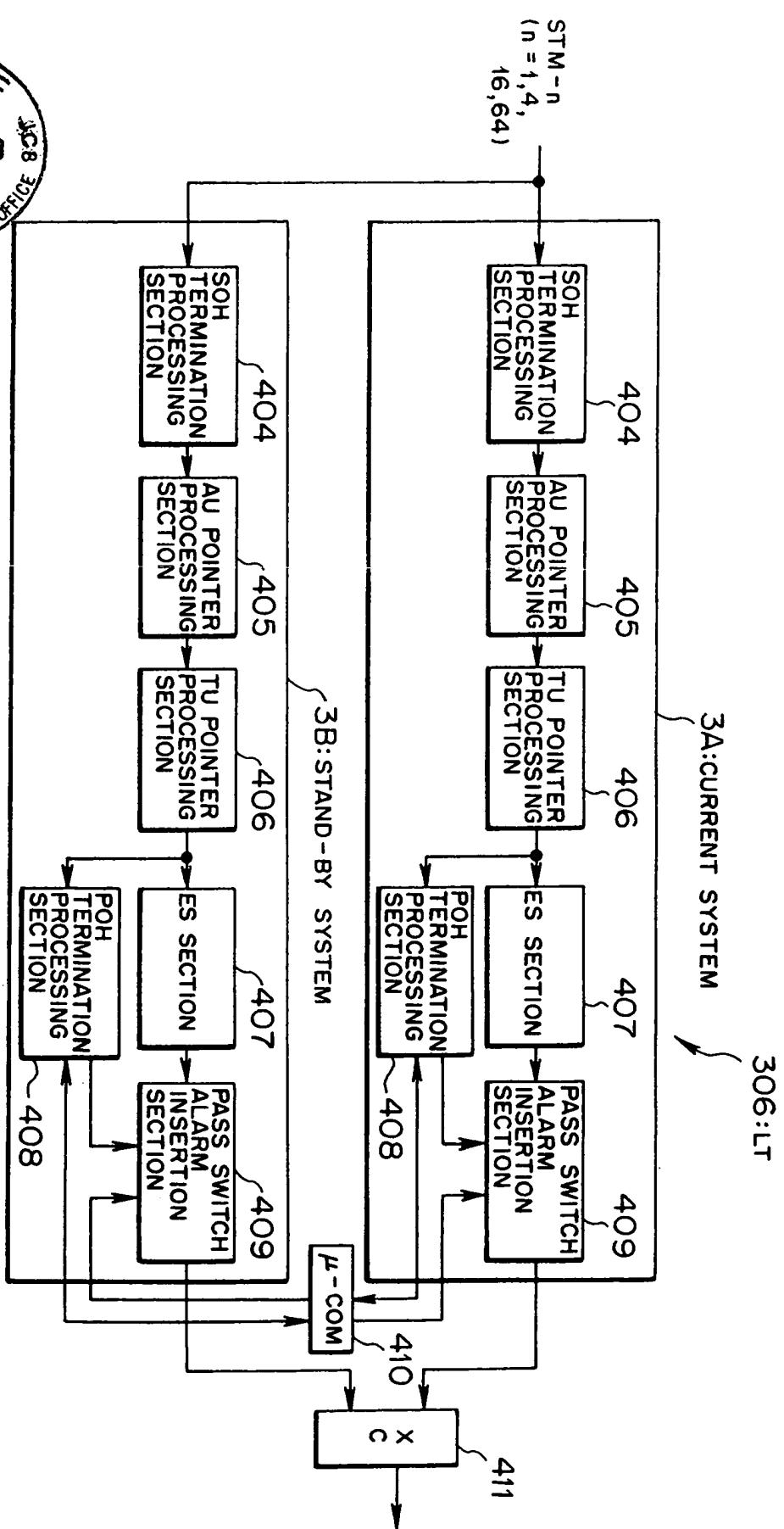
**FIG. 42**  
PRIOR ART



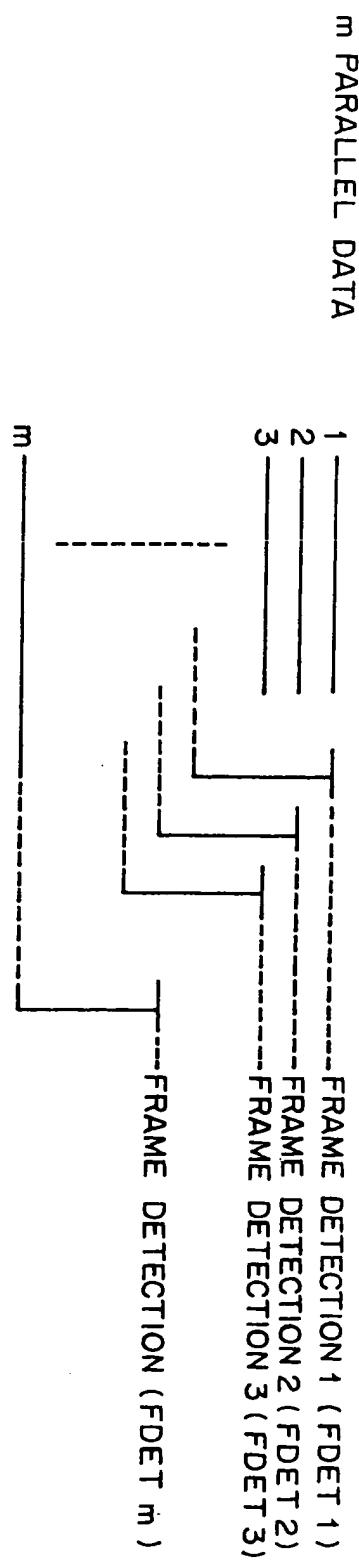
**F | G. 43**  
PRIOR ART



**FIG. 44**  
RELATED ART

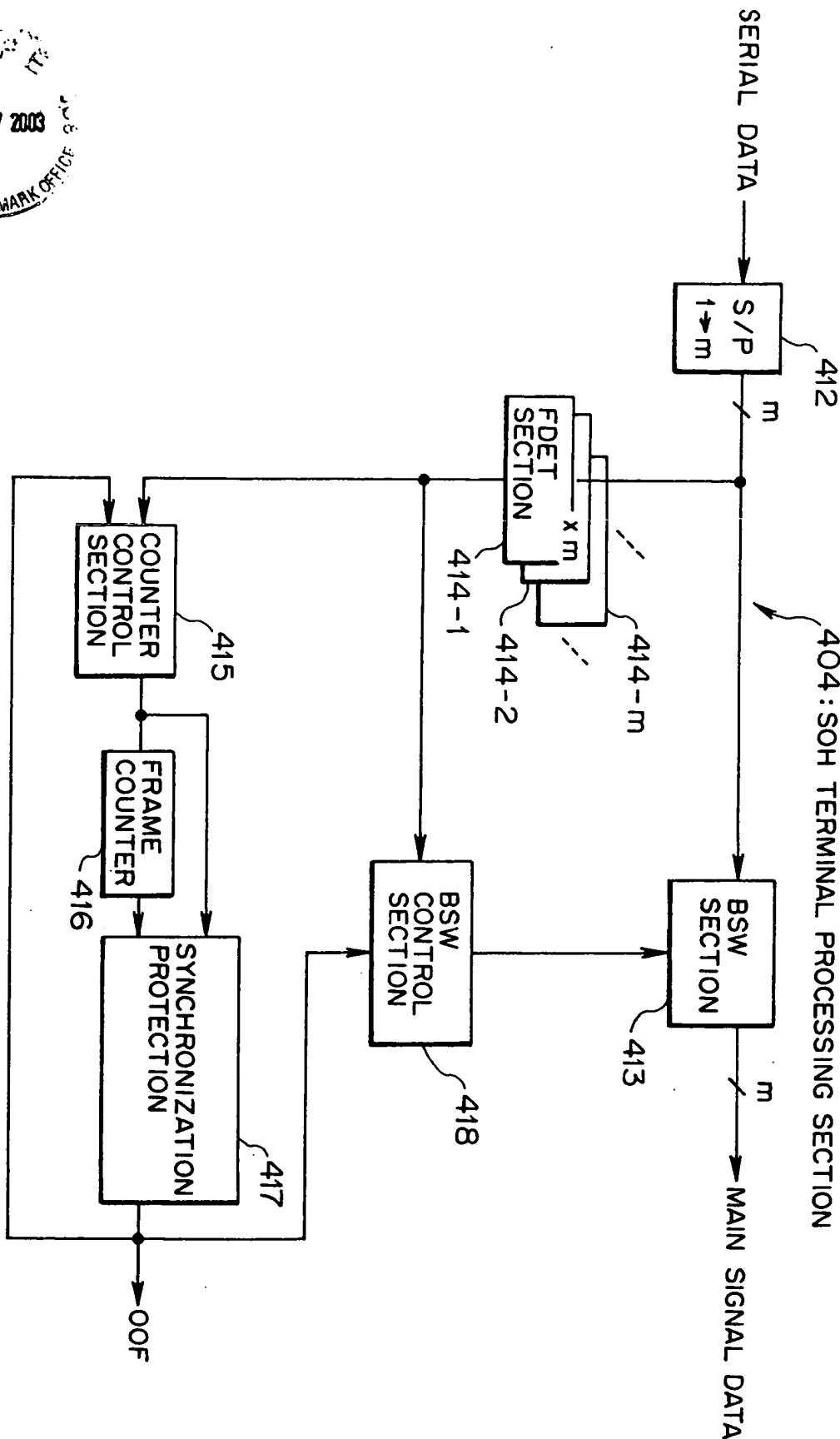


**FIG. 45**  
RELATED ART





## FIG. 46 RELATED ART





**FIG.47**  
RELATED ART



**FIG.48**  
RELATED ART

